Highlights from Hitachi Cambridge Laboratory, UK

In digital logic circuits, binary information is encoded by monitoring the current, on vs. off, through a transistor that serves as a switch. This concept has been extremely effectively scaled over the last decades and led to the exceptionally dense and low cost integrated circuits that we use today. Decreasing the physical size of the component transistors has largely enabled the miniaturization. The reduction in the size of conventional transistors will shortly face the barrier that on the subnano length scale matter is discrete. The atomistic nature of matter leads to variability in device characteristics, which is the major problem in device down-scaling.
As we approach the physical limits of two-dimensional circuits essentially new paradigms are needed to sustain the rate of progress that our society has become used to.

A novel approach to increase the functionality of logic circuits is to introduce single-electron devices in the logic design. Single-electron devices can encode multi-valued logic in the charge, orbital and spin degree of freedom enabling the reduction of circuit elements to perform equivalent logic gates.

From the start of the TOLOP project, we utilized single-electron devices and more particularly single-electron transistors and the novel single-atom transistors (SAT) to perform logic full adder operations [1]. We used the discrete nature of matter at the atomic scale to offer a viable solution to downscaling limitations. Deterministic doping emerges as a technique that overcomes variability problems. Furthermore, single atom doping allows for device functionality that exceeds that of a simple switch. This functionality of single-atom transistors, SATs, is robust due to the strong natural confinement of the Coulomb potential of the dopant. We connect the basic units, the SATs, with gain thereby allowing for a scalable circuit.
It is because of the nature of SATs that our innovative Si device and experimental design can significantly accelerate the transfer of the new paradigm for device architecture from the laboratory to the R&D department.

[1] J.A. Mol et al. PNAS 108 13969 (2011)