Challenges in Energy Efficient Power, Logic and RF/mm-wave Electronics

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Overview

In an ICT system, there are 3 important aspects

- Powering the system
- Processing information in the system
- Communicating information within and beyond the system

Silicon Compatible GaN Power Electronics
The UK "PowerGaN" Consortium

A £6.2M EPSRC Programme Grant, commenced 1st March 2013

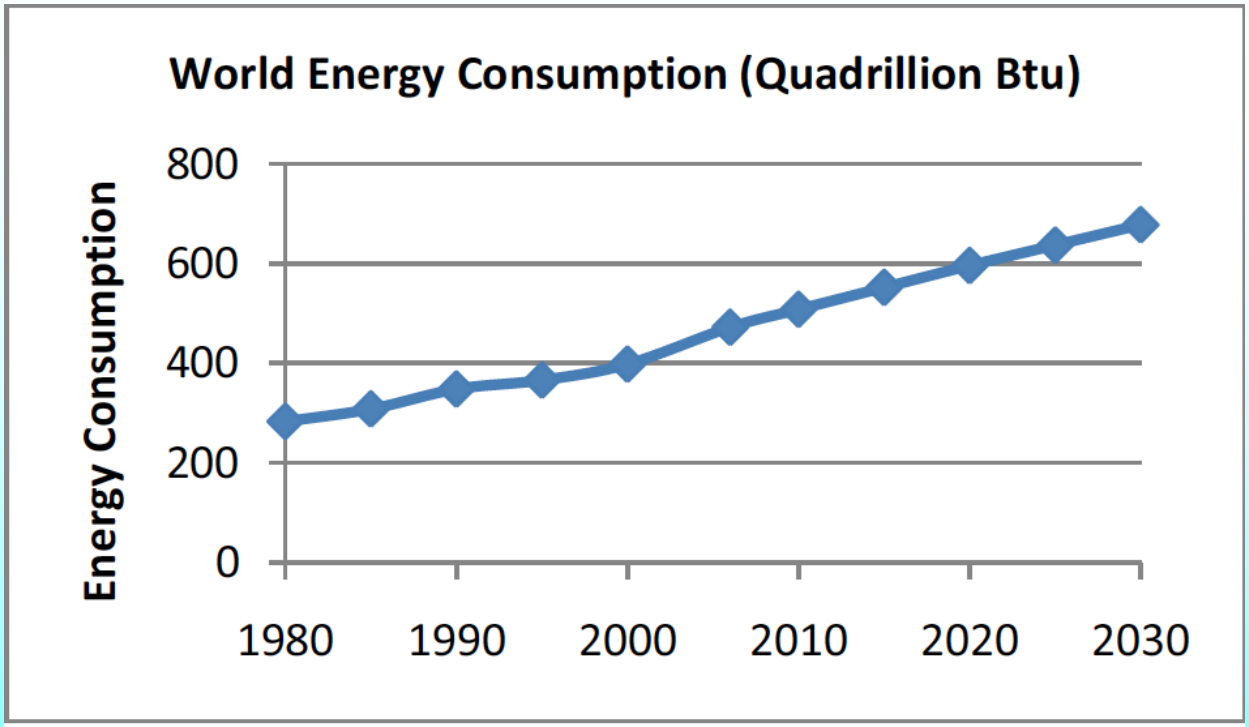
An "associated project" to the £18M UK Centre for Power Electronics

7 Universities
12 Industrial Collaborators

33 strong research team

University of BRISTOL · UNIVERSITY OF CAMBRIDGE · University of Glasgow · UNIVERSITY OF LIVERPOOL · MANCHESTER 1824 The University of Manchester · The University of Nottingham UNITED KINGDOM · CHINA · MALAYSIA · The University Of Sheffield.

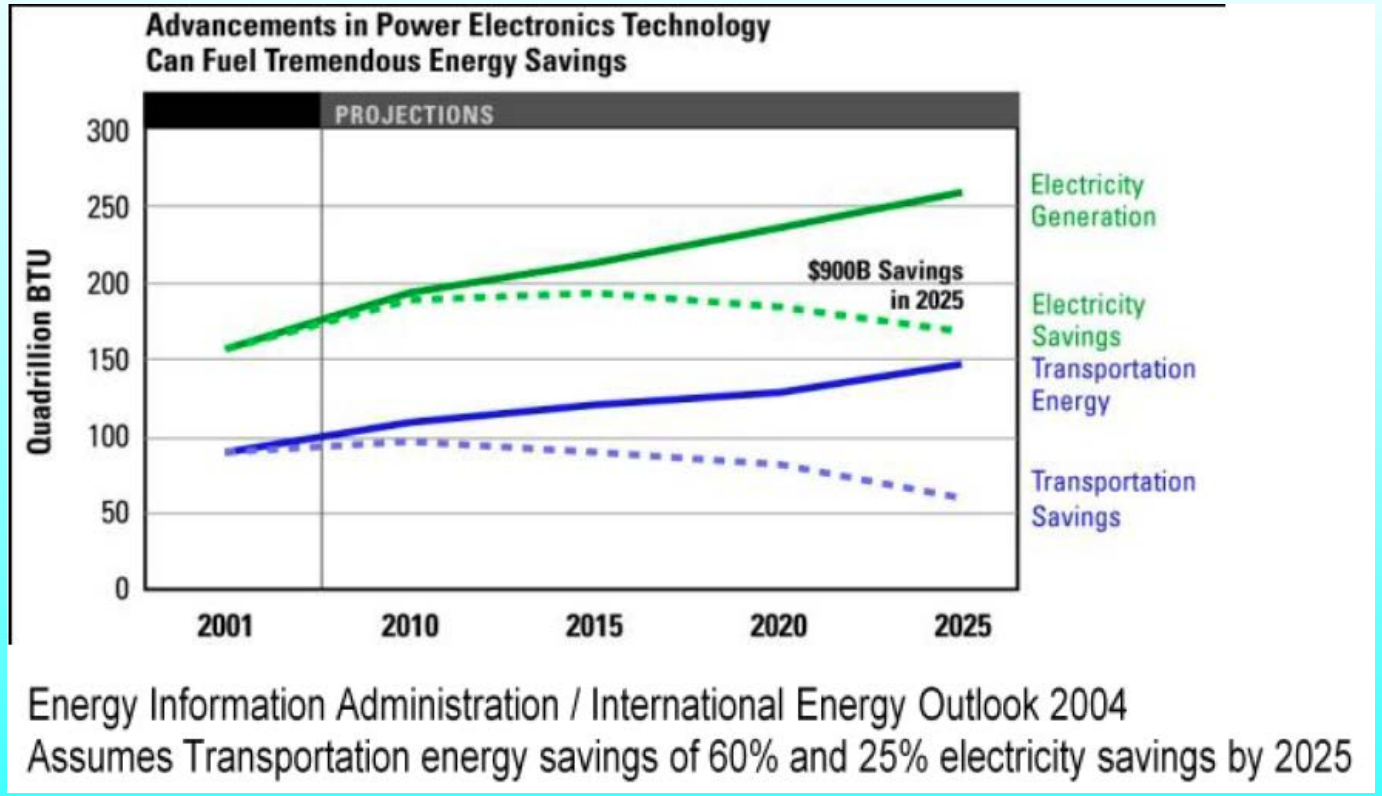
The Challenge



Using existing power conversion solutions, total global energy consumption is predicted to increase by 35% over the next 20 years.

One Significant Solution

Based on the intrinsic properties of GaN, future generations of power electronics components have the potential to reduce worldwide energy consumption by up to 25 %



Energy Information Administration / International Energy Outlook 2004
Assumes Transportation energy savings of 60% and 25% electricity savings by 2025

So, what are these intrinsic properties ?

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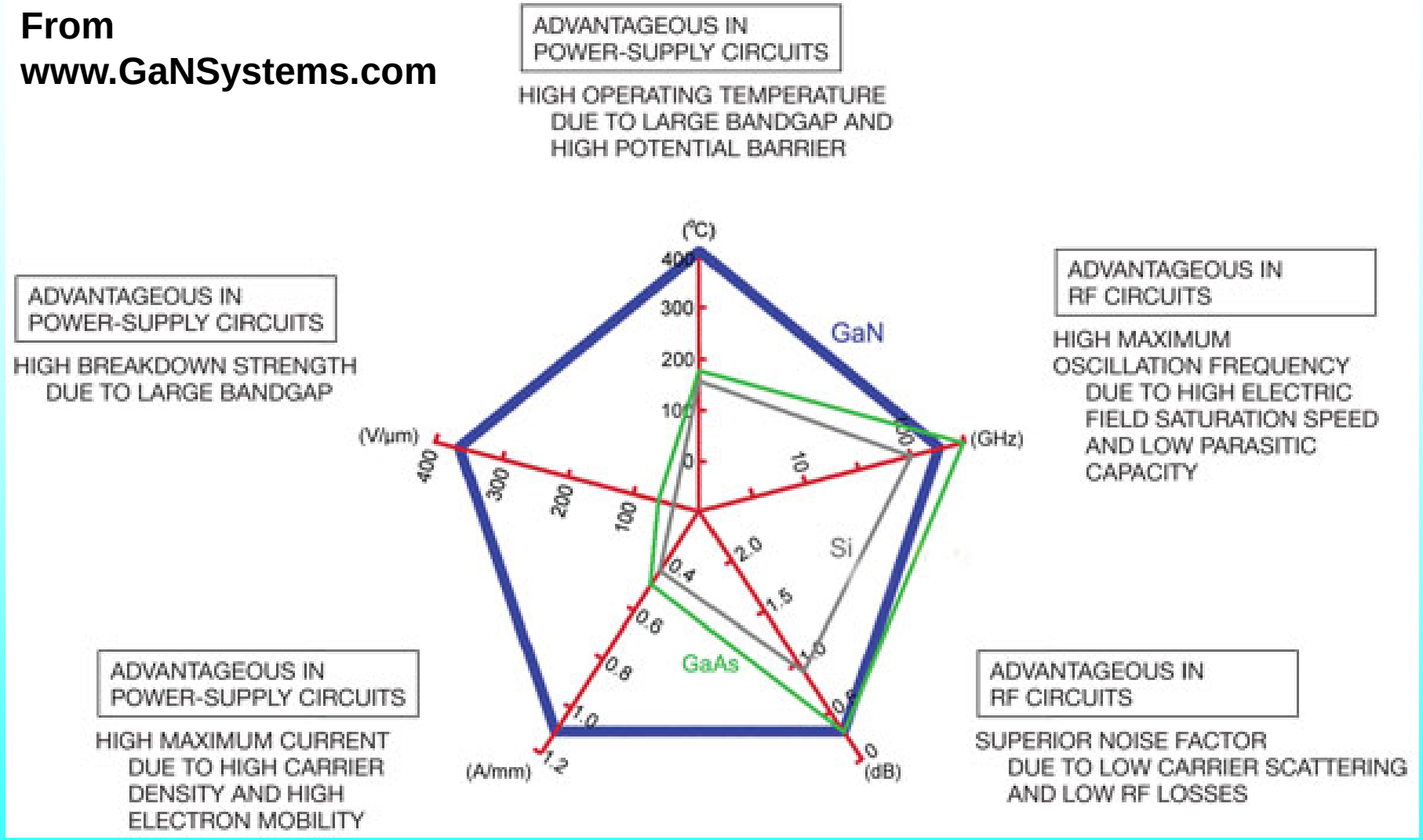
From www.GaNSystems.com



Applications

12% energy saving in transportation
(motors in electric vehicles, trains etc)

20% energy saving in consumer electronics
(permanent magnet motors etc)

8% energy saving in lighting
(in combination with GaN LEDs)

20% energy saving in IT infrastructure
(power distribution in server farms etc)

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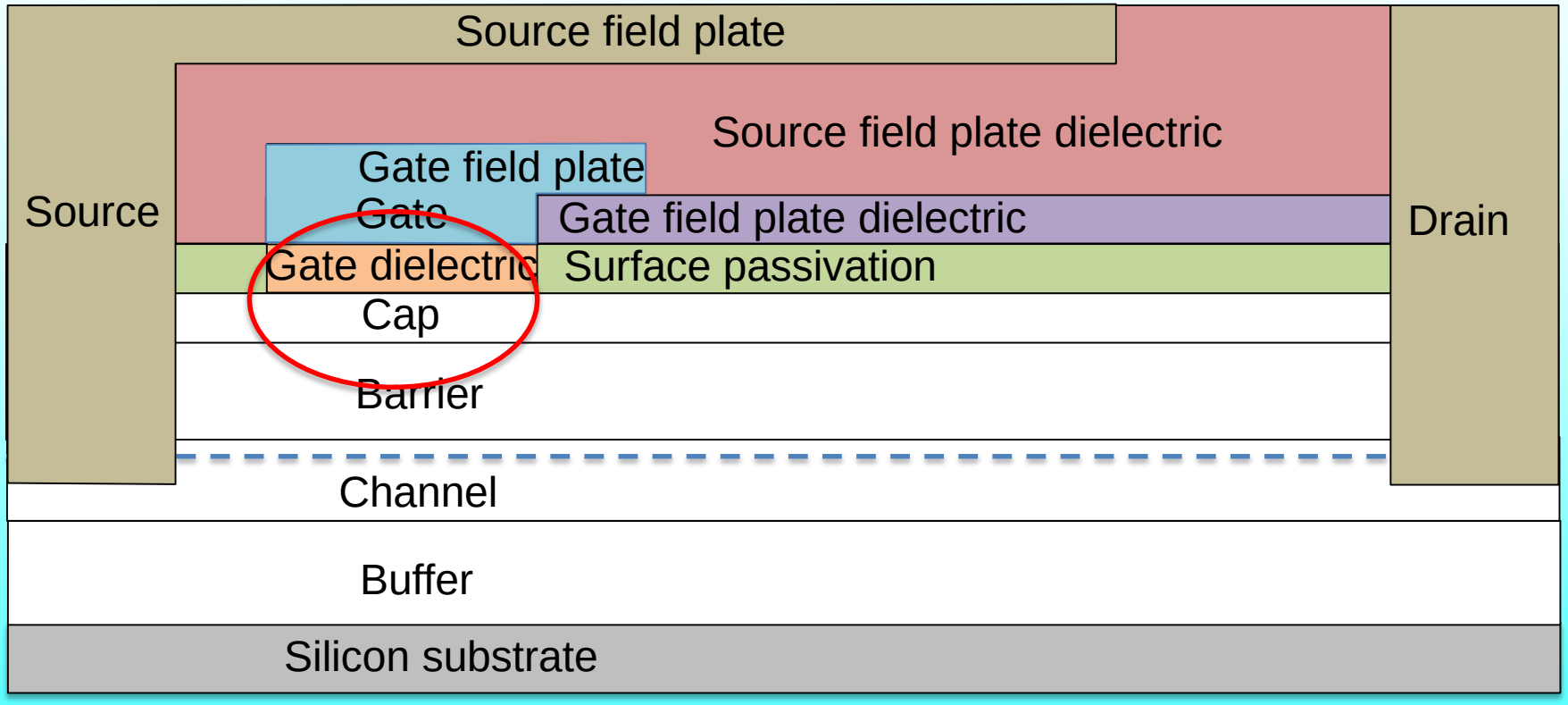
Why Silicon Compatible GaN Power Electronics ?

- Global market in GaN power electronics will be $1-10B by 2020
- But this will only happen with widespread (>90%) adoption
- Cost has to be less than ~$3 / cm^2 chip area
- Requires at least 10 million 150 mm wafer starts per annum
- Has to be silicon based

Some of the issues under investigation…..



Cap layer choices - GaN, AlInN

Gate dielectric – Al_2O_3, SiN – V_{th}, hysteresis, D_{it}

GaN Interface and Surface studies

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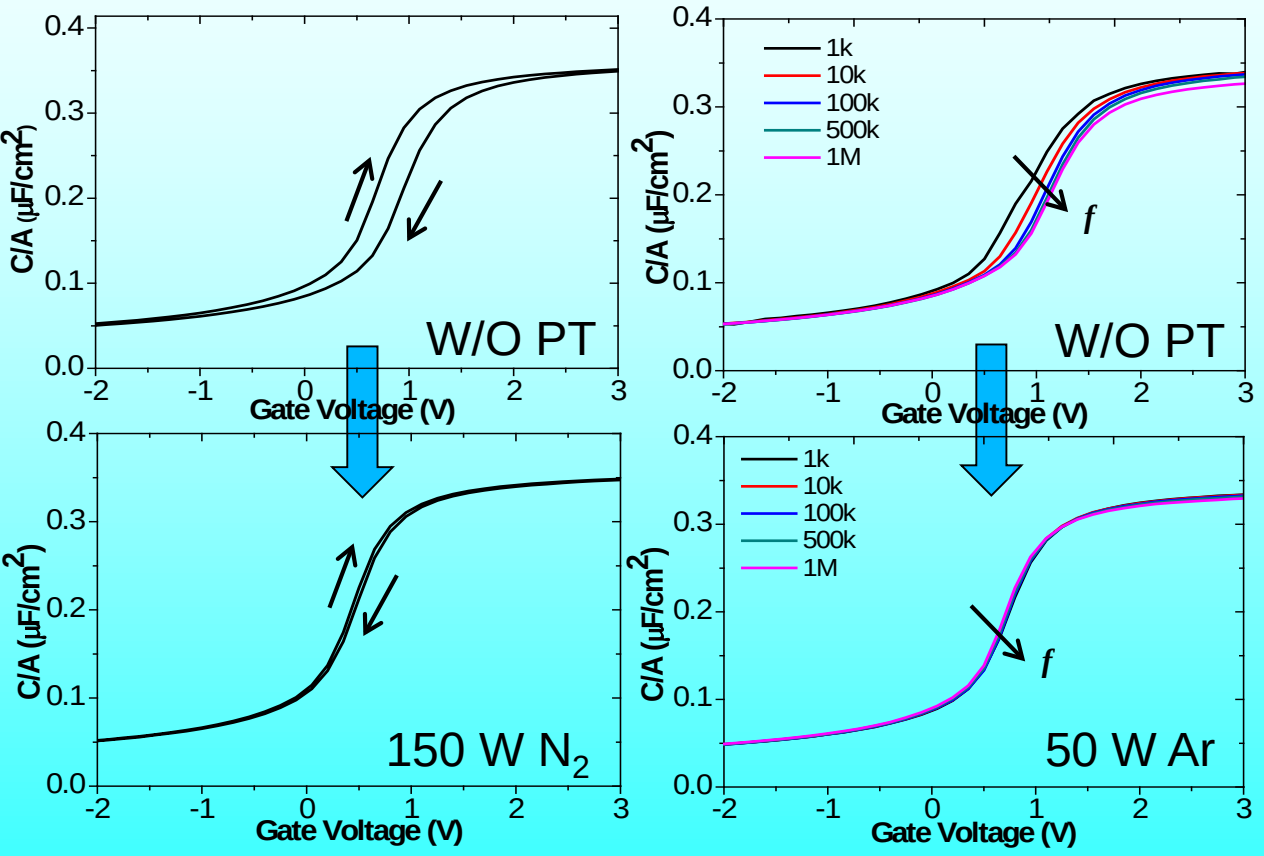
- GaN MOSCAP devices used for wet/dry ex-situ/in-situ surface modification studies (ongoing)
- HCl and KOH ex-situ wet cleaning, passivation of surface using NH_4F and $(NH_4)_2S$, in-situ plasma cleaning using N_2, O_2 and Ar plasmas at different plasma powers



Hysteresis (10 kHz, V_G= -5 V to 5 V)

Frequency dispersion (1 kHz to 1 MHz)

	Frequency dispersion (△mV)	Lowest D_{it} (cm^{-2} eV^{-1})
Control (No PT)	310	1.64×10^{13}
50 W Ar	35	5.05×10^{10}
KOH 62% / H_2O / HCl 40% / H_2O	134	6.28×10^{11}

Stress test (10 kHz) repeat measure: $V_{G\,min}$ = -5 V, $V_{G\,max}$= 0 V to 5V (step = 0.5 V)		
	Hysteresis V_G= -5 V to 5 V (△mV)	Flat band voltage shift $V_{G\,max}$= 0 V to 5V (△mV)
Control (No PT)	272	220
150 W N_2	34	20
KOH 62%/H_2O/HCl 40%/H_2O	48	30

All plasma pretreatment samples showed improvement compared to control sample.

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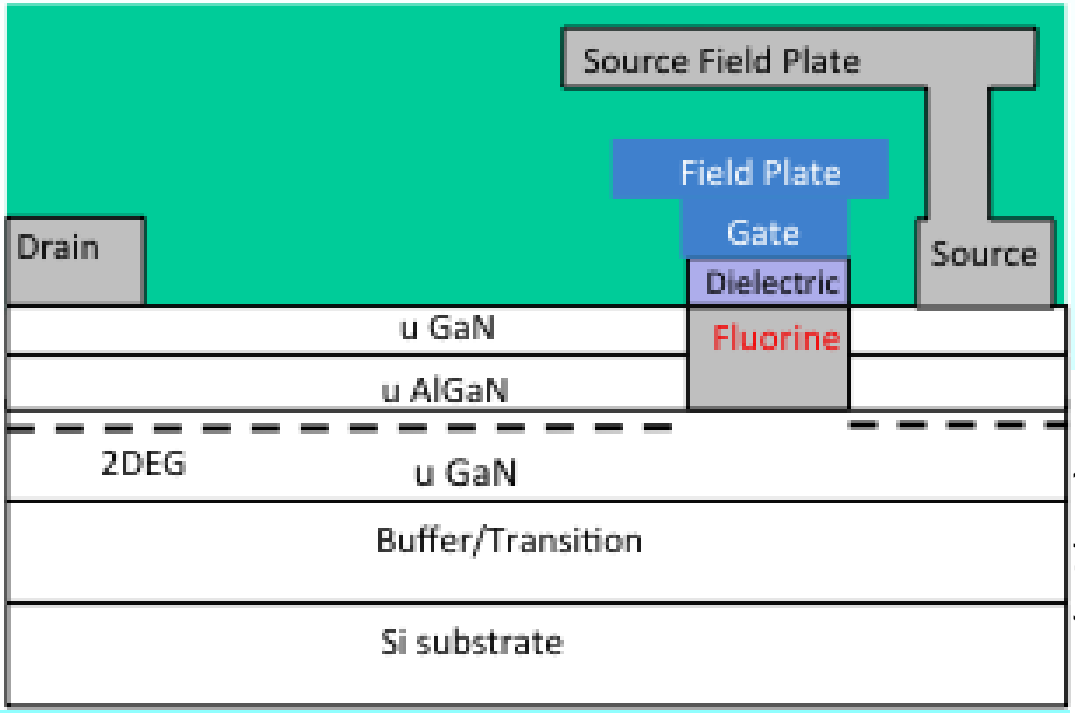
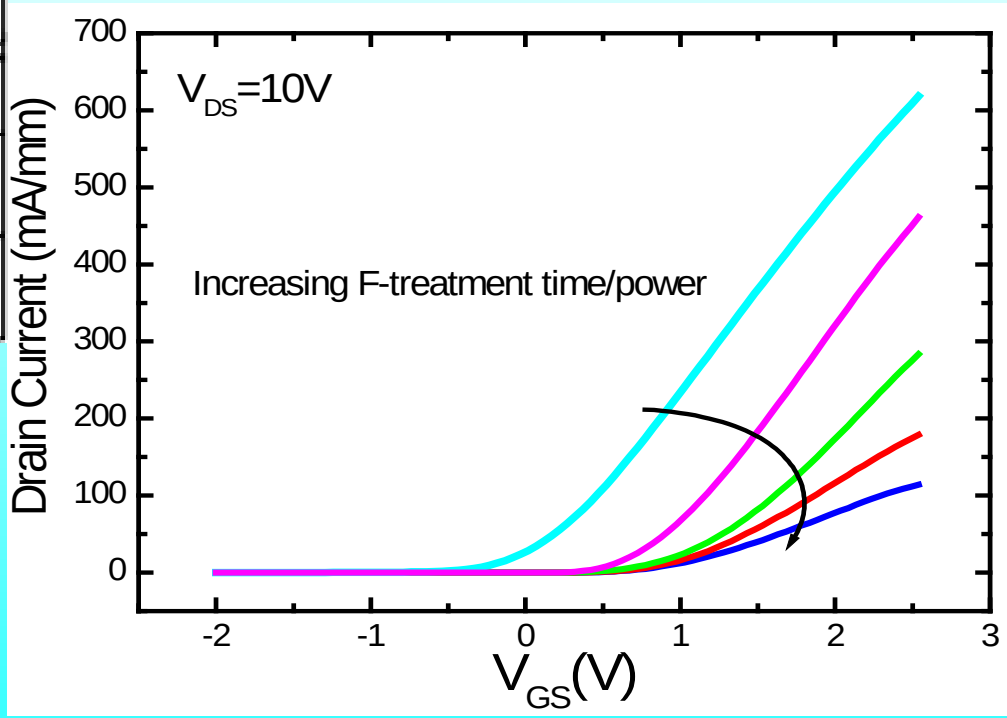
Ex-situ flourine plasma treatment using CHF_3 RIE





AlInN/GaN HFET

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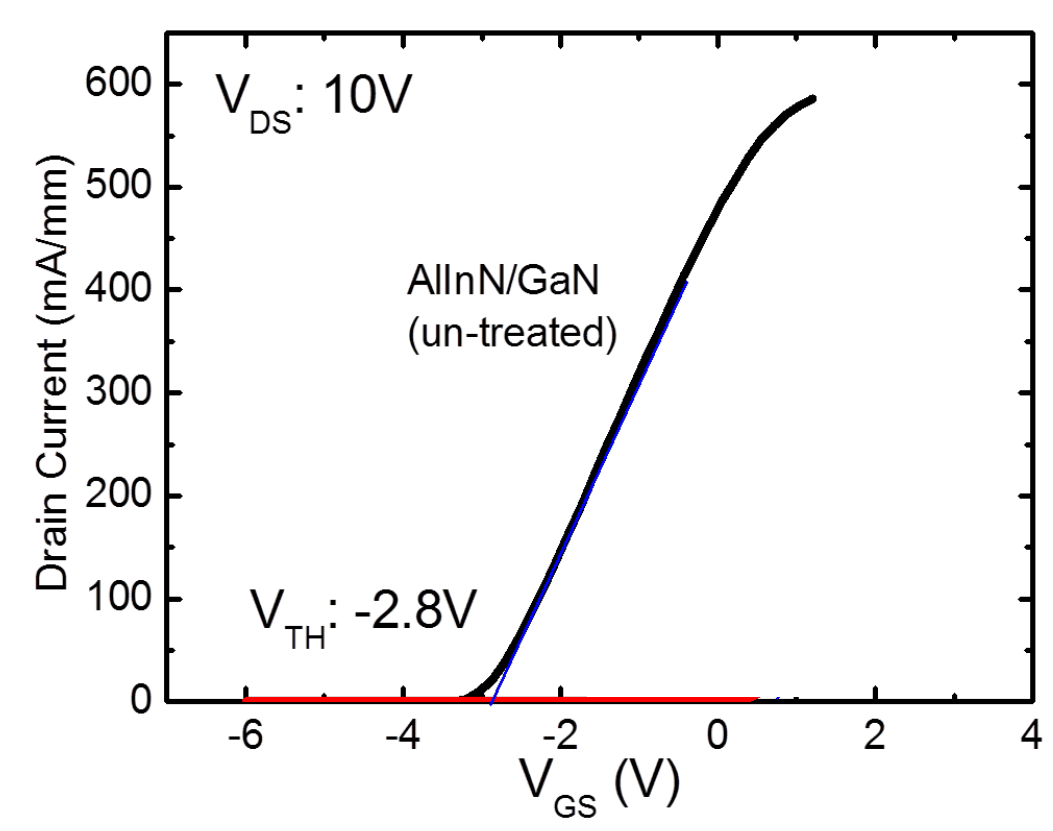
GaN (2nm)
AlInN (11nm)
AlN (1nm)
UID GaN (250nm)
Carbon-doped GaN (1800nm)
Compositionally graded AlGaN (850nm)
AlN (250nm)
Si substrate



Normally on – Depletion mode transistor

2DEG density (Hall): ~$8 \times 10^{12} cm^{-2}$

Mobility (Hall): ~$1400 cm^2 V^{-1} s^{-1}$

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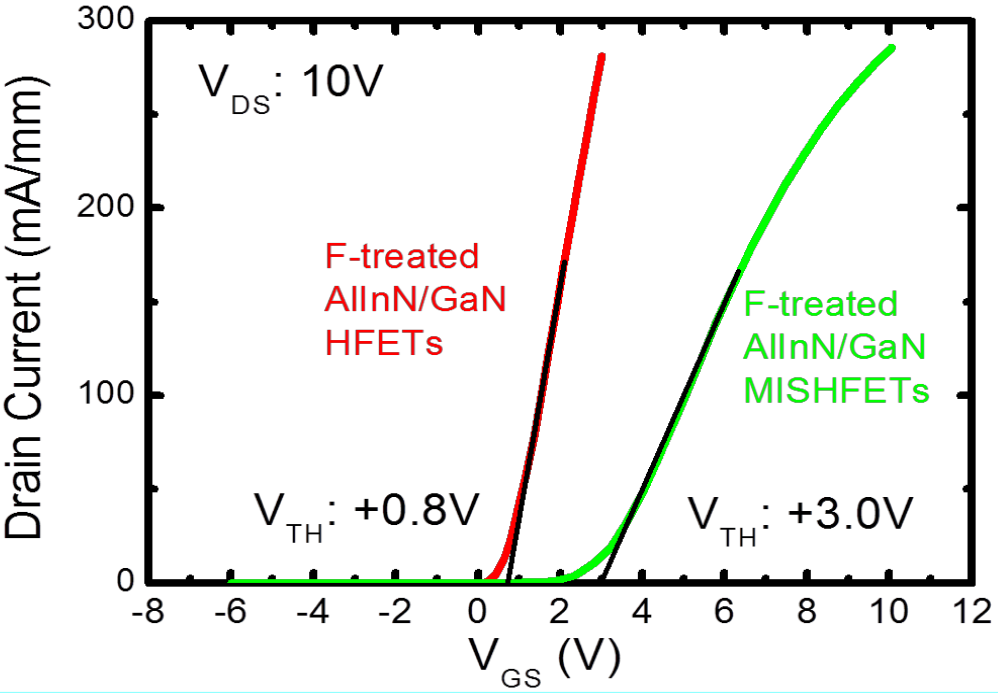
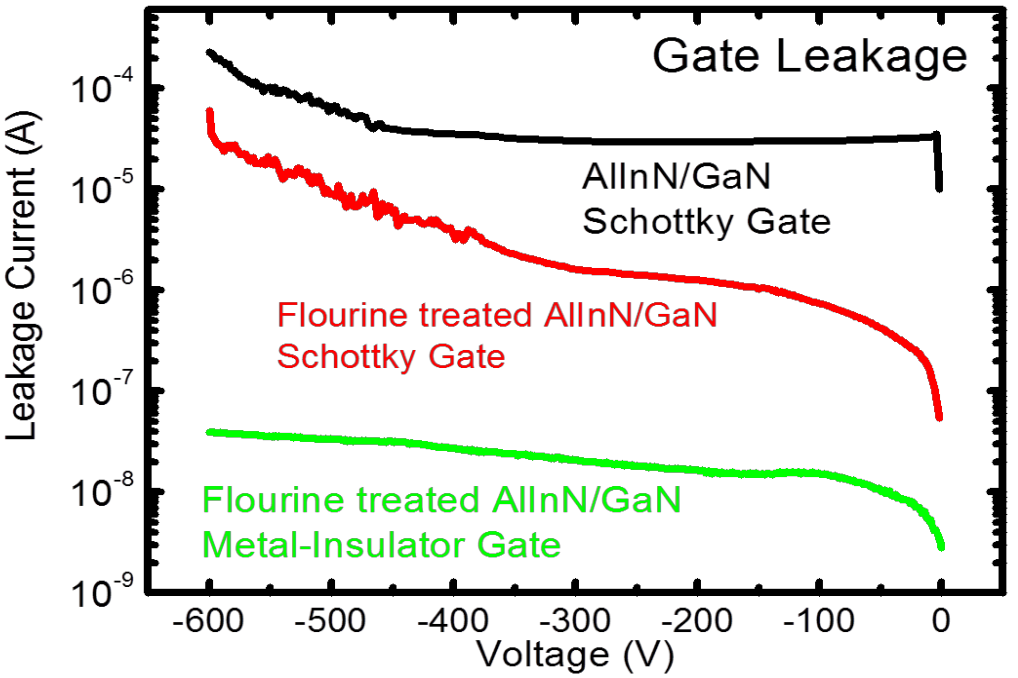
F plasma shifts V_{TH} and reduces gate leakage





F treatment shifts V_{TH} to +0.8V

Gate leakage is dominated by bulk leakage (via AlInN barrier)

F plasma increases barrier height – reduces gate leakage

20nm SiNx gate dielectric further reduces gate leakage current

Shifts V_{TH} more positive

With suitable buffer structure, can extend breakdown voltage

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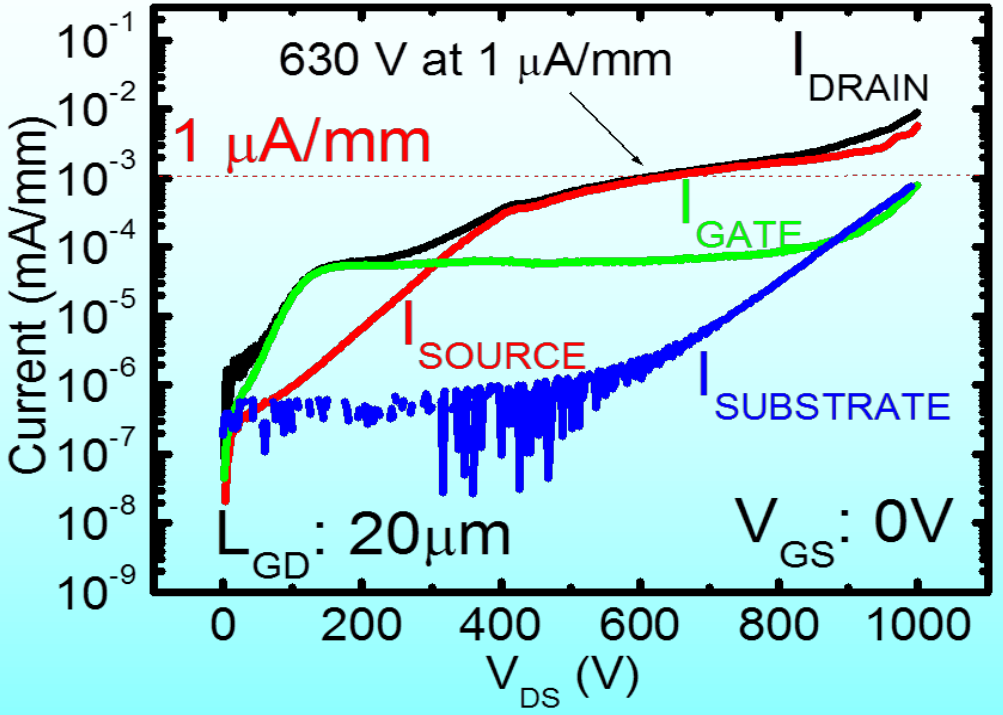
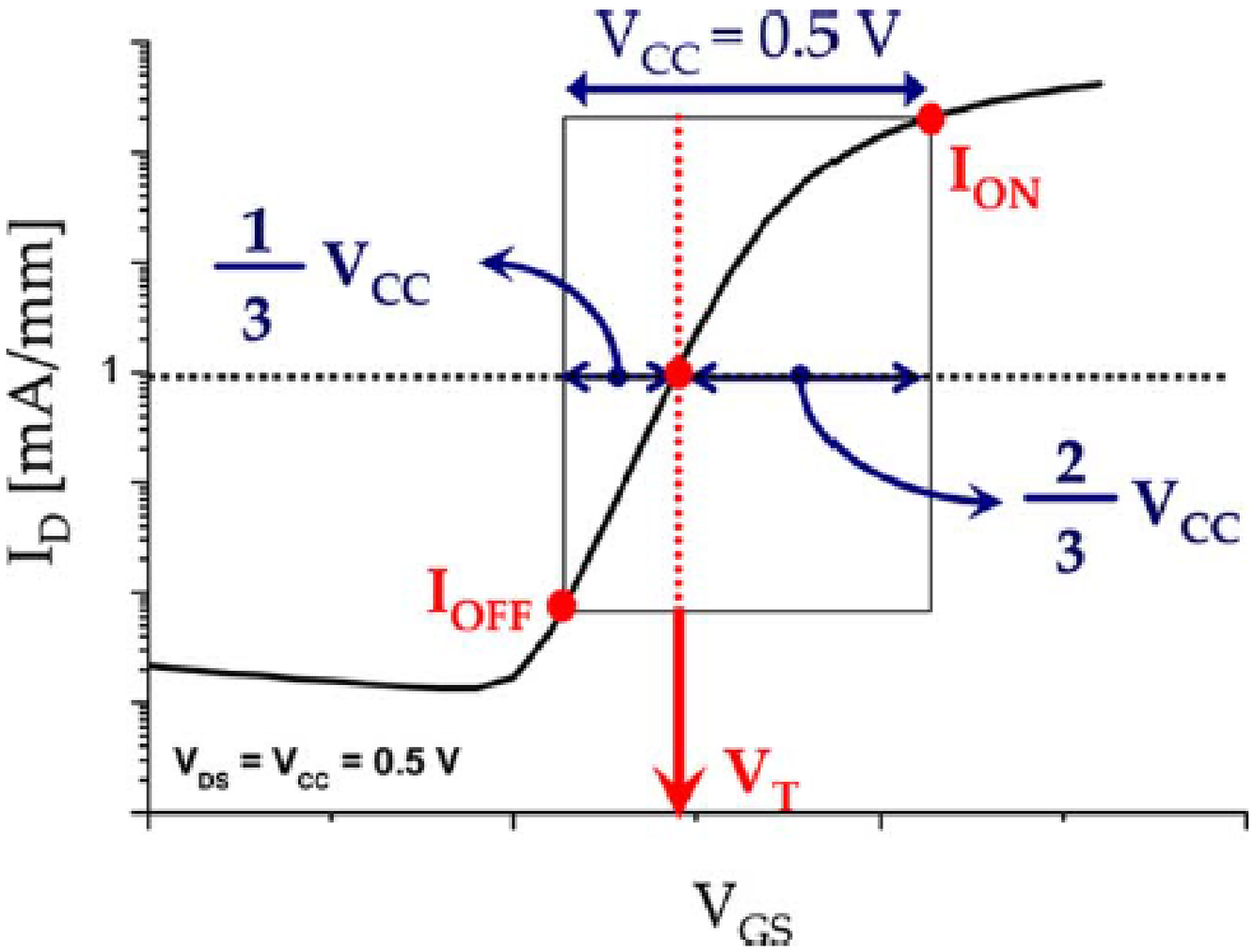
GaN (2nm)
AlInN (11nm)
AlN (1nm)
UID GaN (250nm)
Carbon-doped GaN (1800nm)
Compositionally graded AlGaN (500nm)
AlN (12nm)
Carbon-doped GaN (1800nm)
Compositionally graded AlGaN (500nm)
AlN (12nm)
Carbon-doped GaN (1800nm)
Compositionally graded AlGaN (850nm)
AlN (250nm)
Si substrate



Blocking voltage of 600V at leakage of 1μA/mm and 1kV at leakage of 10μA/mm

Processing information in the System - Logic



For a given supply voltage :

Define I_{OFF} (eg 100 nA/mm)
Then determine I_{ON}

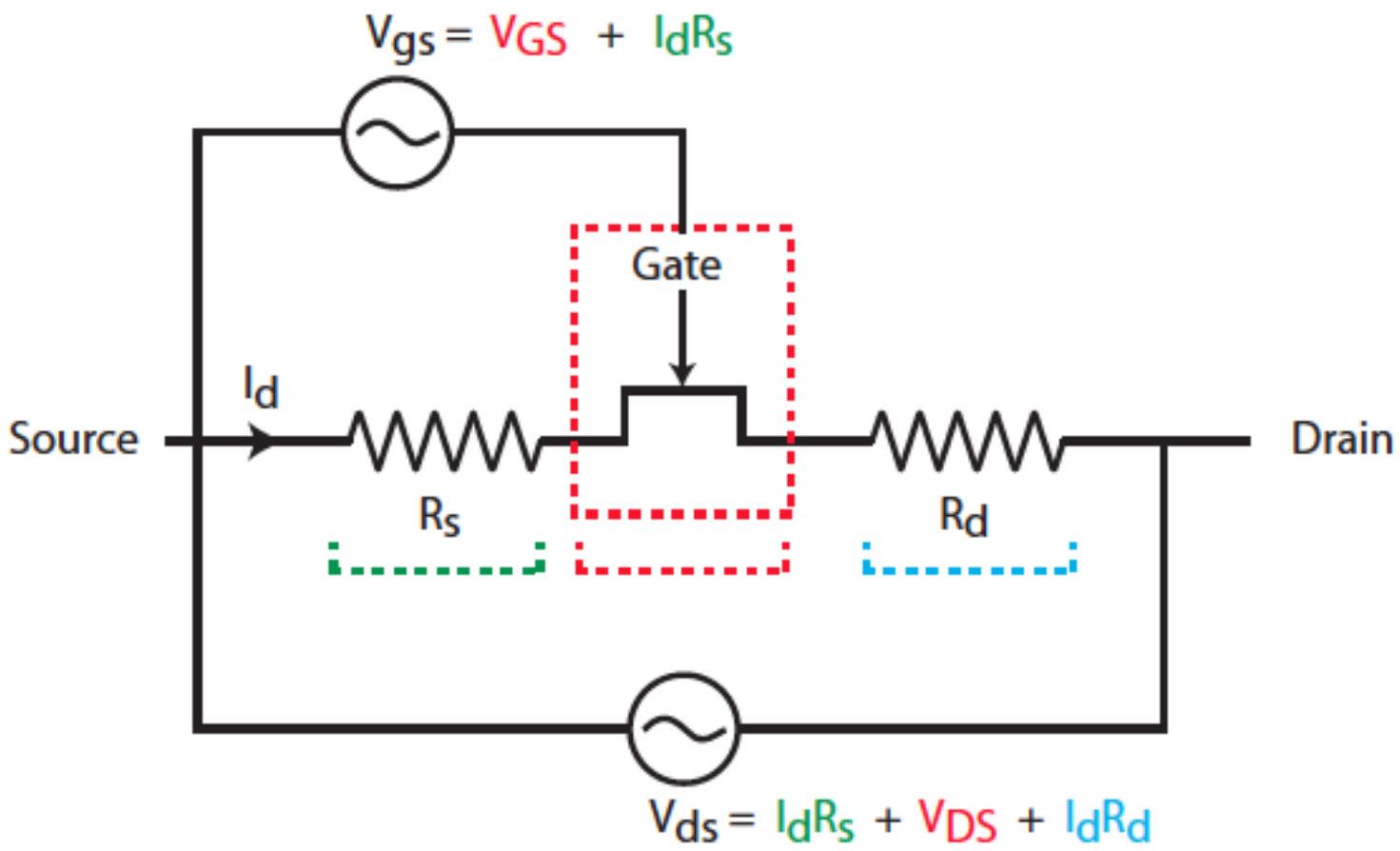
Key thing is how much current swing can be achieved for a given supply voltage

On-state – Impact of Source Resistance

Intrinsic transconductance

$$g_{m0} = \frac{\delta I_{ds}}{\delta V_{gs}}$$

$$V_{gs} = V_{GS} + I_d R_s$$



$$g_m = \frac{\delta I_{ds}}{\delta(V_{GS} + I_d R_s)}$$

$$= \frac{\delta I_{ds}}{\delta V_{GS} + \delta I_d R_s}$$

$$= \frac{\frac{\delta I_{ds}}{\delta V_{GS}}}{1 + \frac{\delta I_d}{\delta V_{GS}} R_s}$$

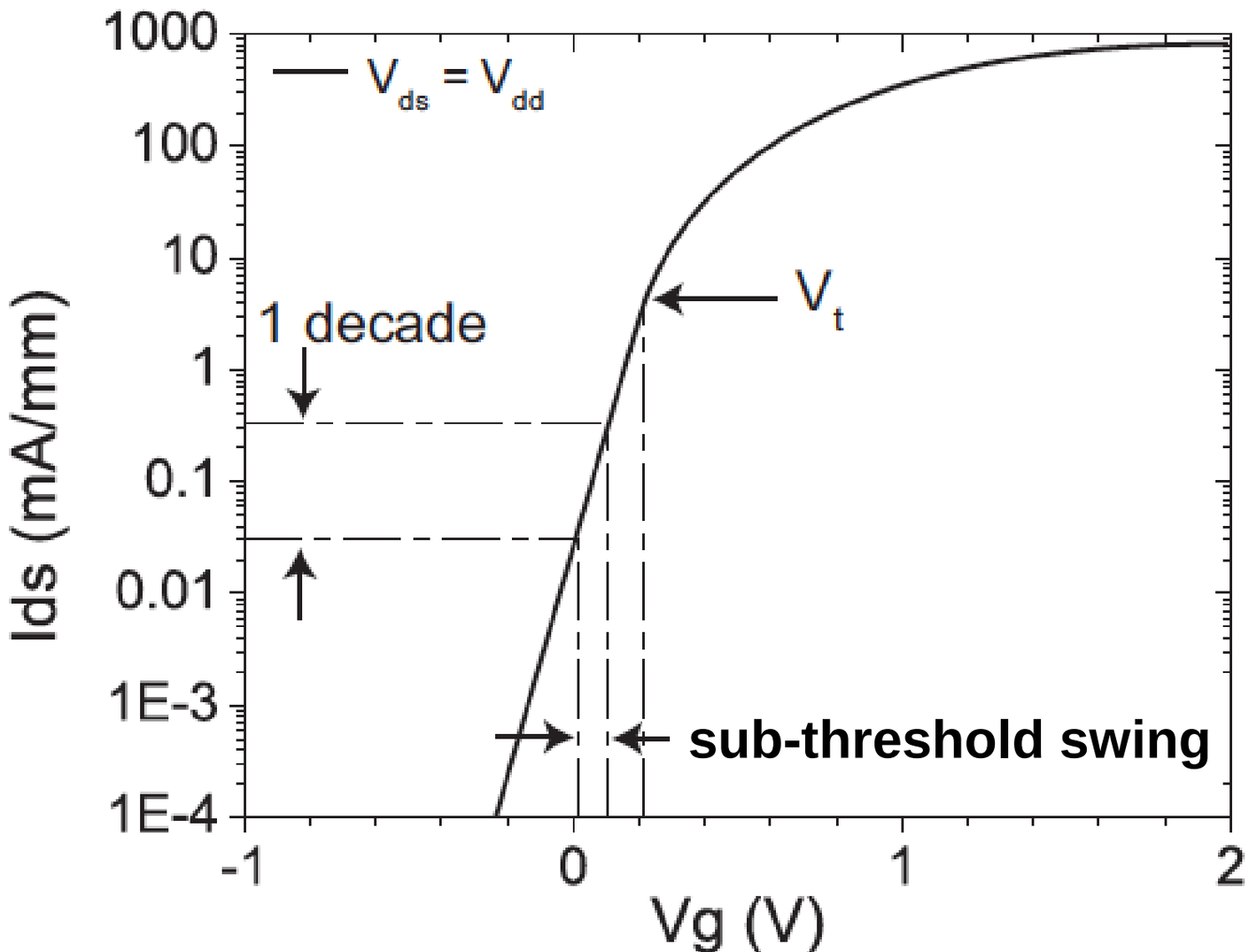
$$= \frac{g_{m0}}{1 + g_{m0} R_s}$$

So, in the on-state, when there is significant current flowing, the source resistance needs to be minimised so that available gate voltage is used “efficiently”

Off-state – Sub-threshold swing

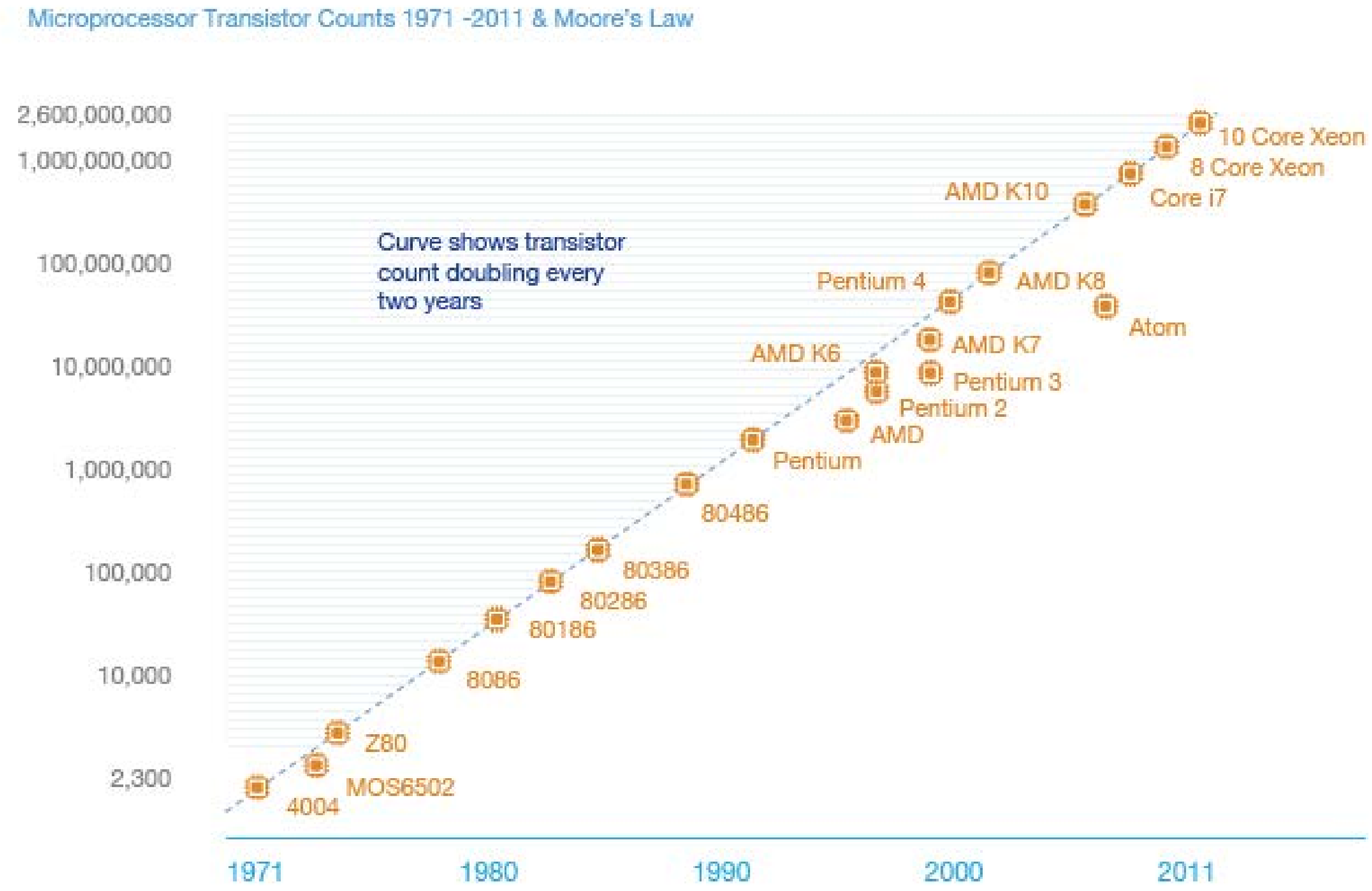
In the off-state, have to "use" gate voltage to switch device off.
In the ideal case, it can be shown that sub-threshold swing,

$$S = \frac{k_B T}{q} \ln(10) \sim 60 mV / decade$$



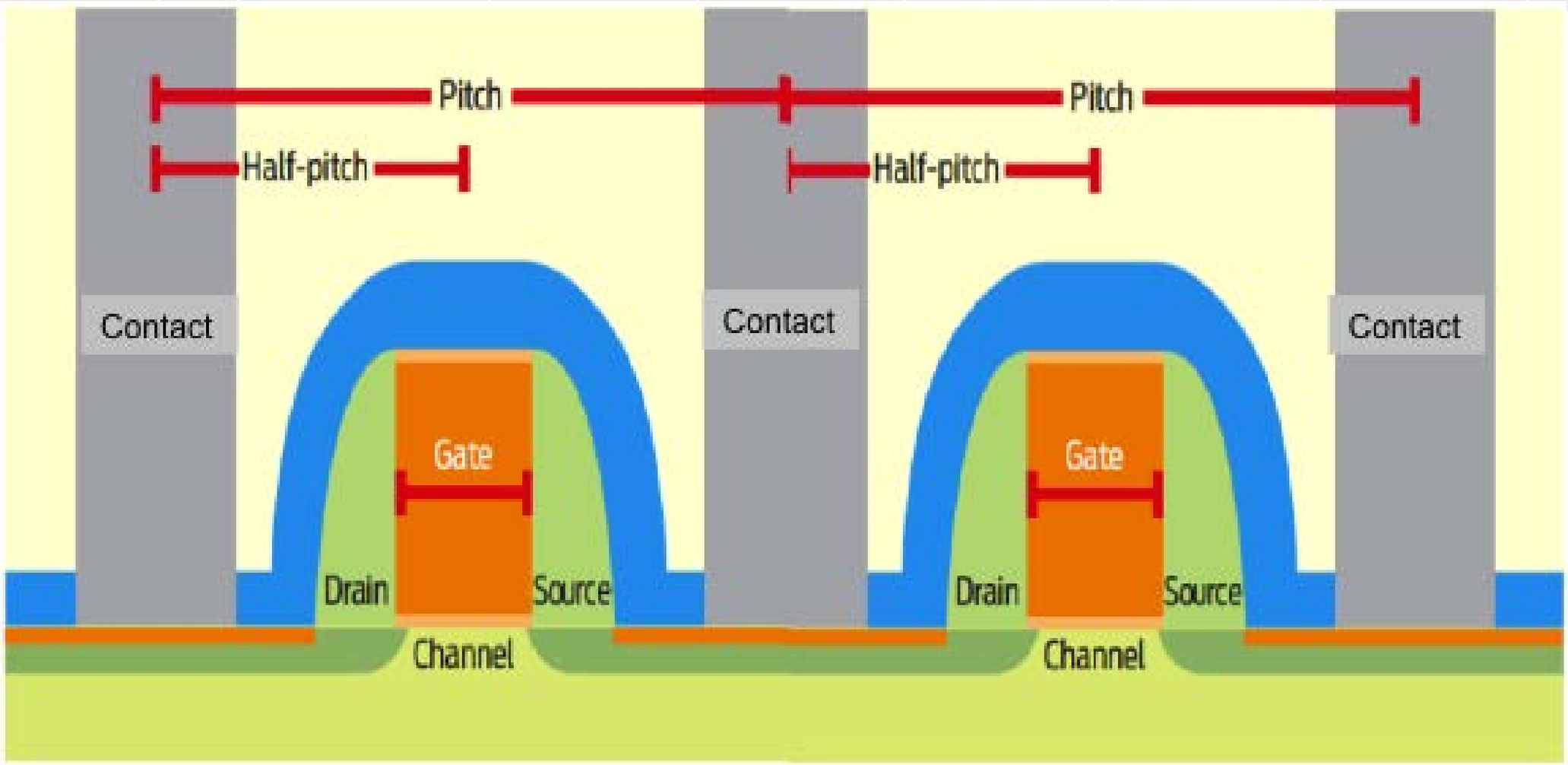
If the gate oxide is not ideal, have to "waste" gate voltage modulating things like charge in the oxide, and so sub-threshold swing increases

Density scaling is driving the industry

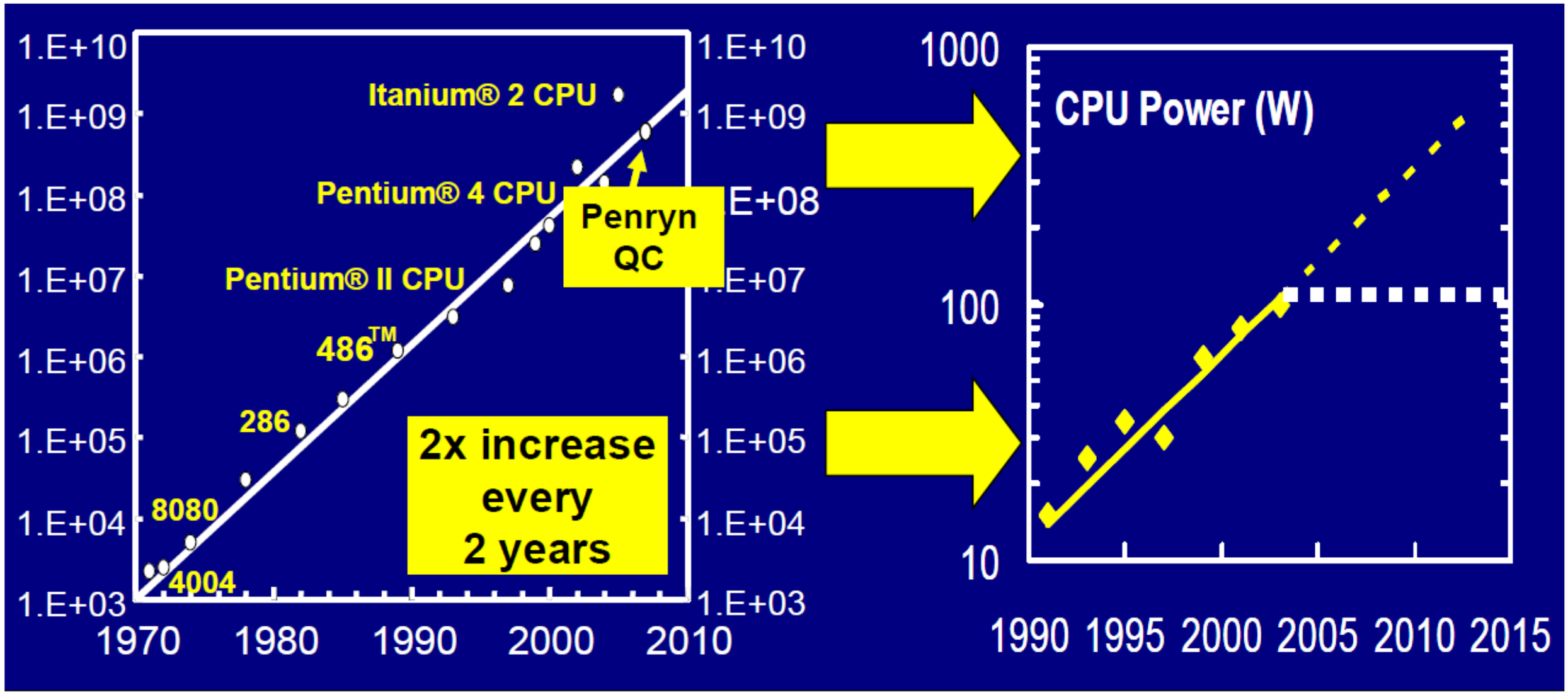


What does this actually mean in practice……..

Year	2011	2015	2018	2019	2020	2024
Gate Pitch (nm)	75	42	30	27	24	15
Physical gate length (nm)	24	17	13	12	11	7



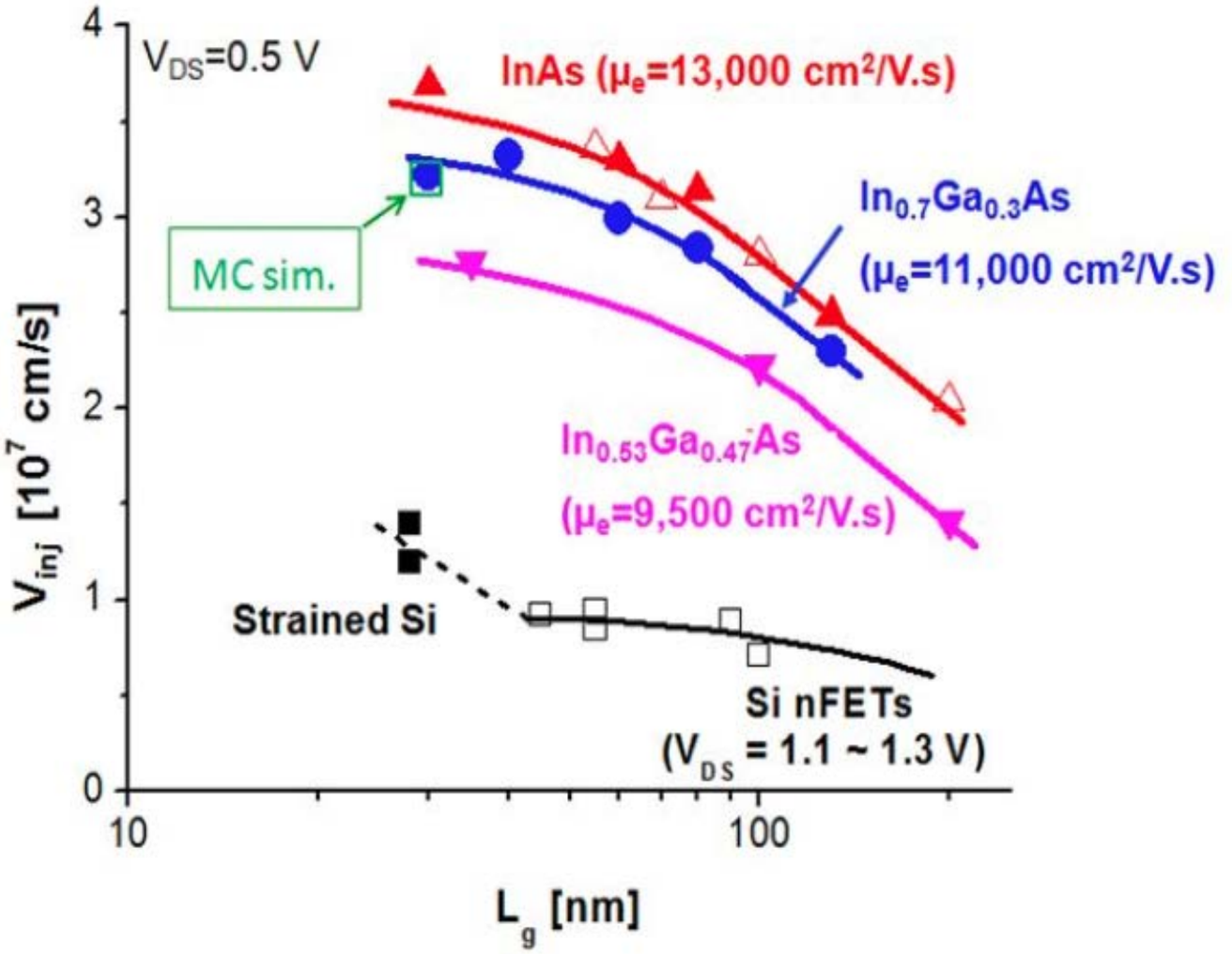
We are living in interesting times……



Power consumption increases with
Clock Frequency; Number of transistors on the chip; (Supply Voltage)^2

?? How to reduce power consumption without impacting performance

High velocity carriers at low voltage

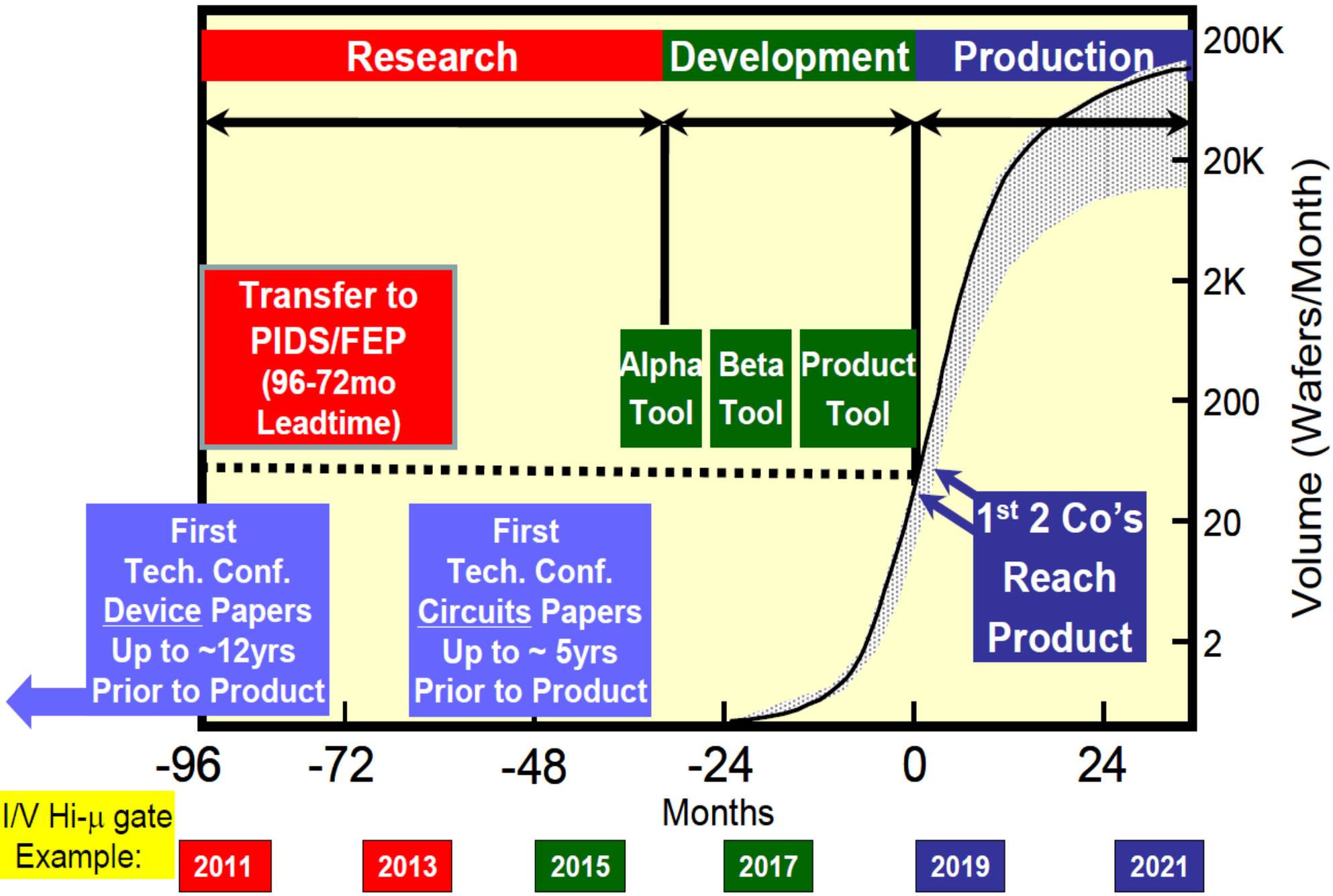


Experimentally determined injection velocity from III-V High Electron Mobility Transistors (not MOSFETs though) compared to Si CMOS

Kim et al – MIT - Proc. IEDM 09

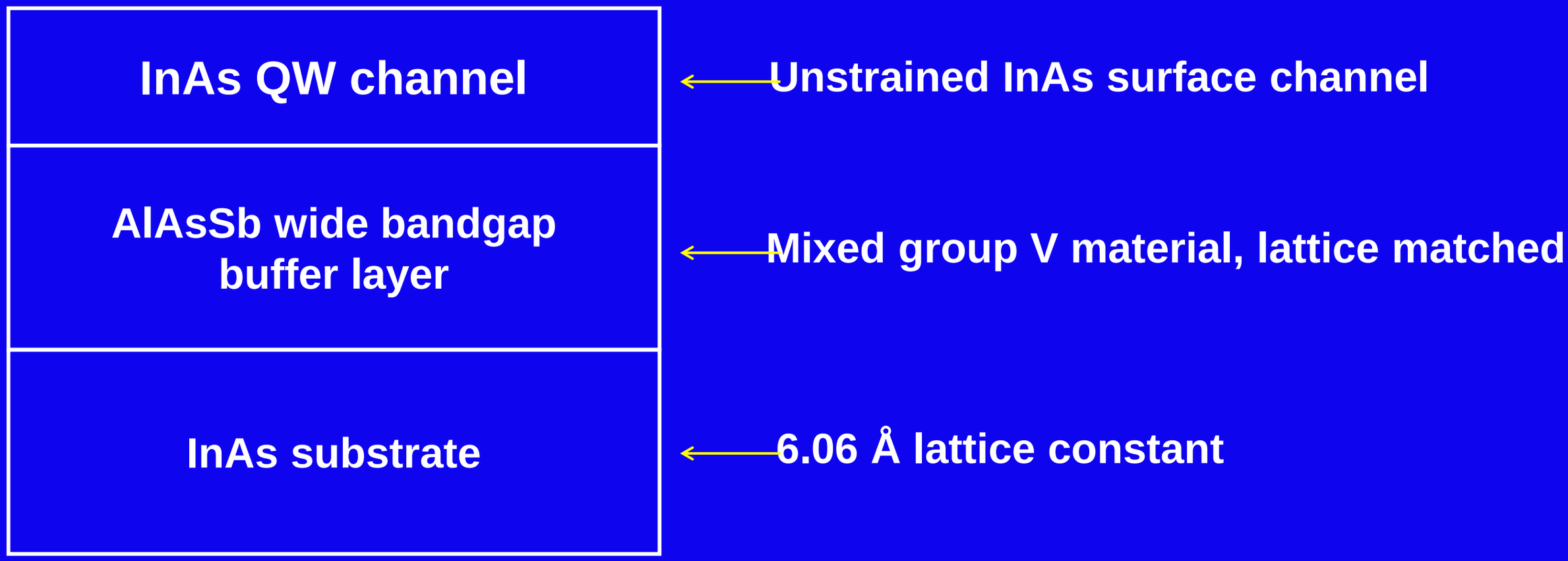
	Si	GaAs	InGaAs	InAs
Bandgap (eV)	1.12	1.43	0.74	0.35
Electron Mobility (cm^2/Vs)	~800	8500	14000	25000

III-V for Continued CMOS Scaling

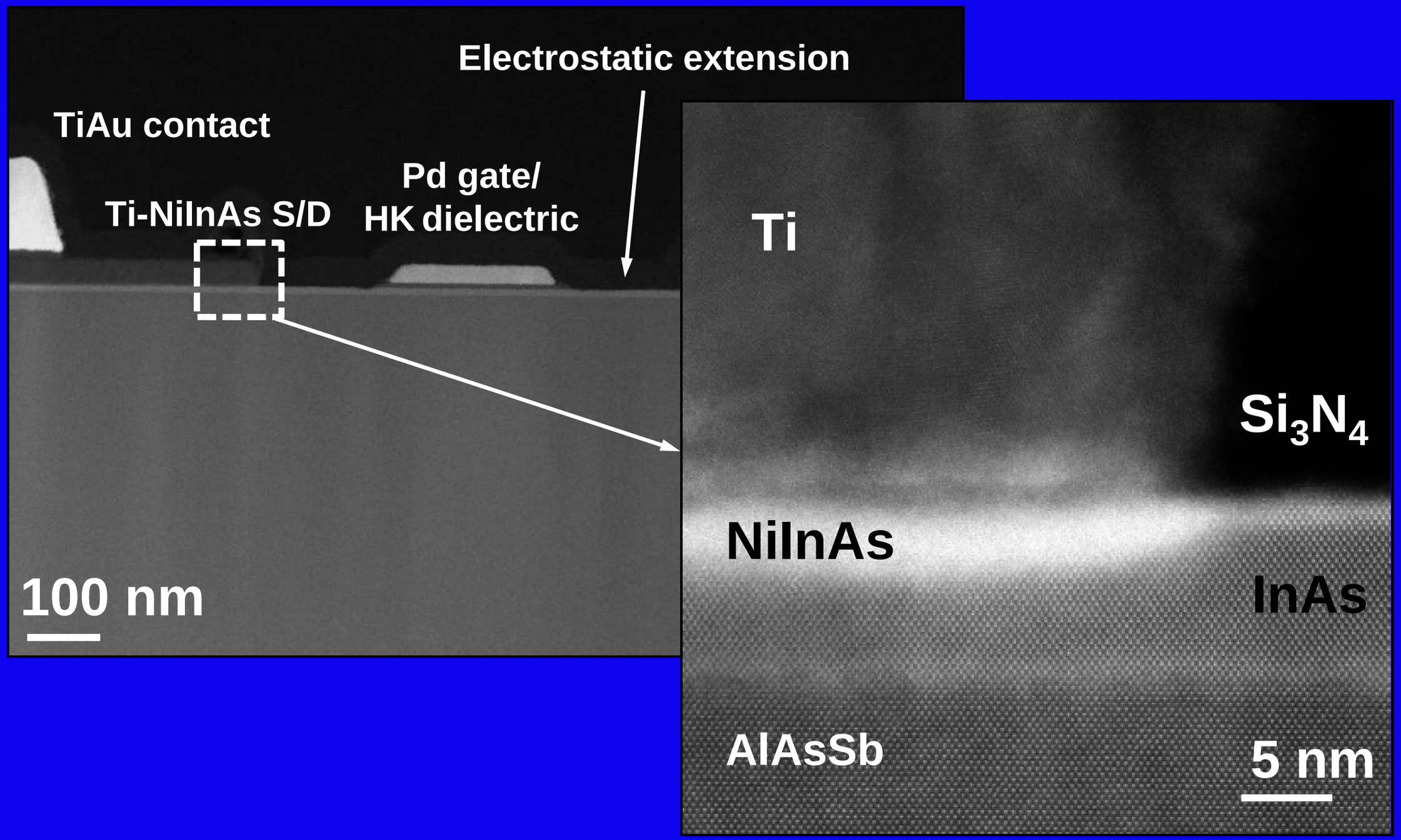


Taken from ITRS Roadmap

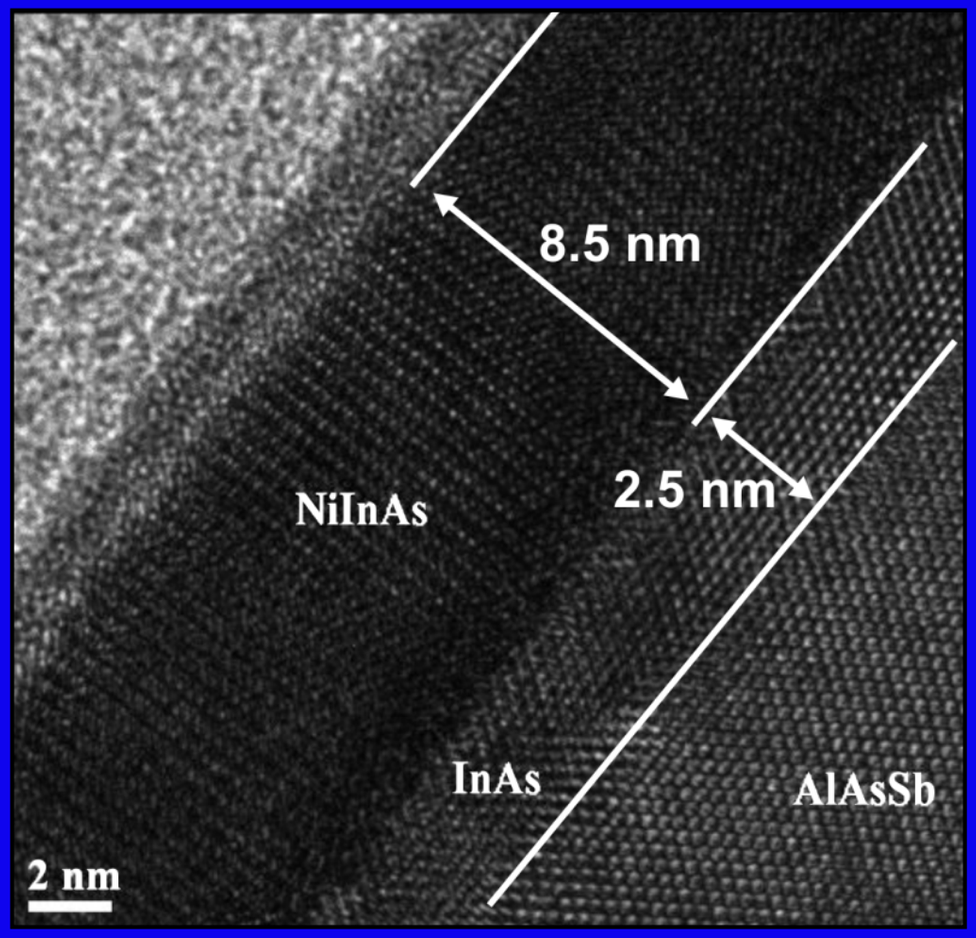
InAs N-MOSFET device demonstrator

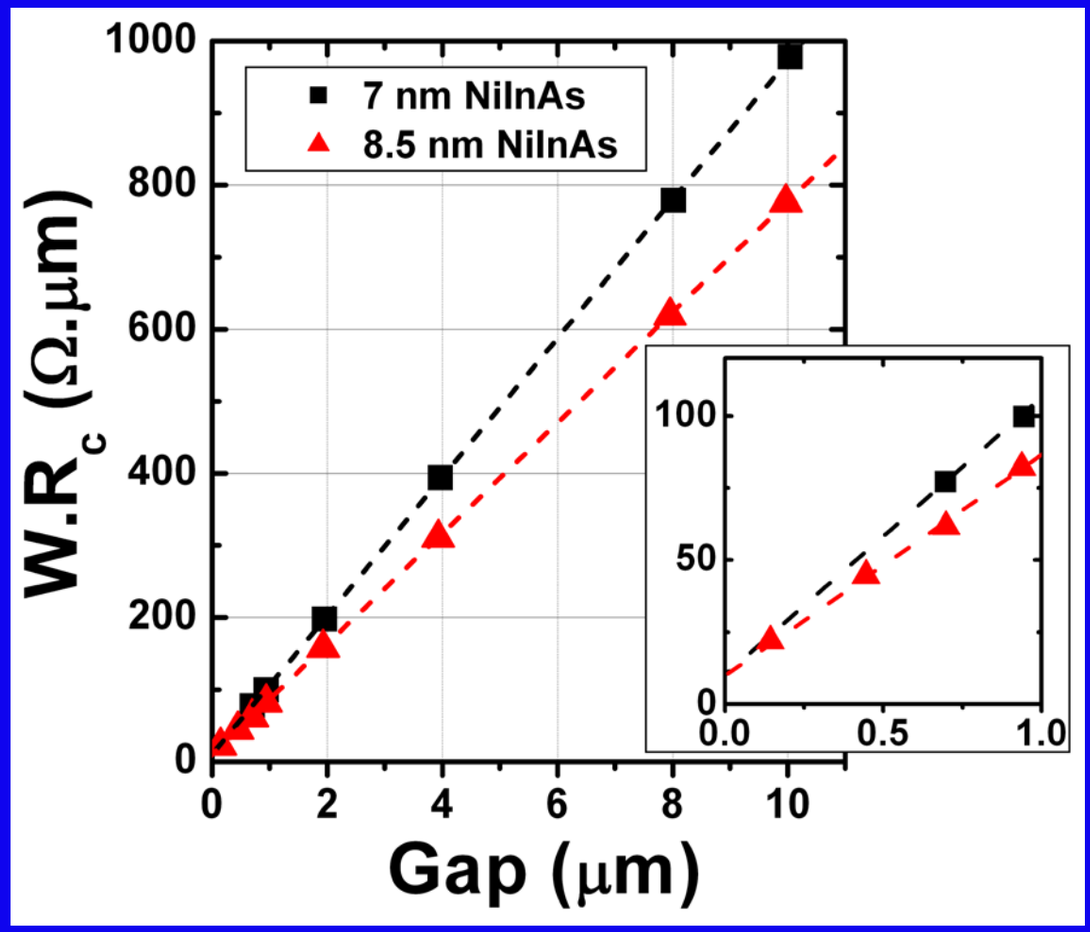


TEM cross-section



Source/drain contacts



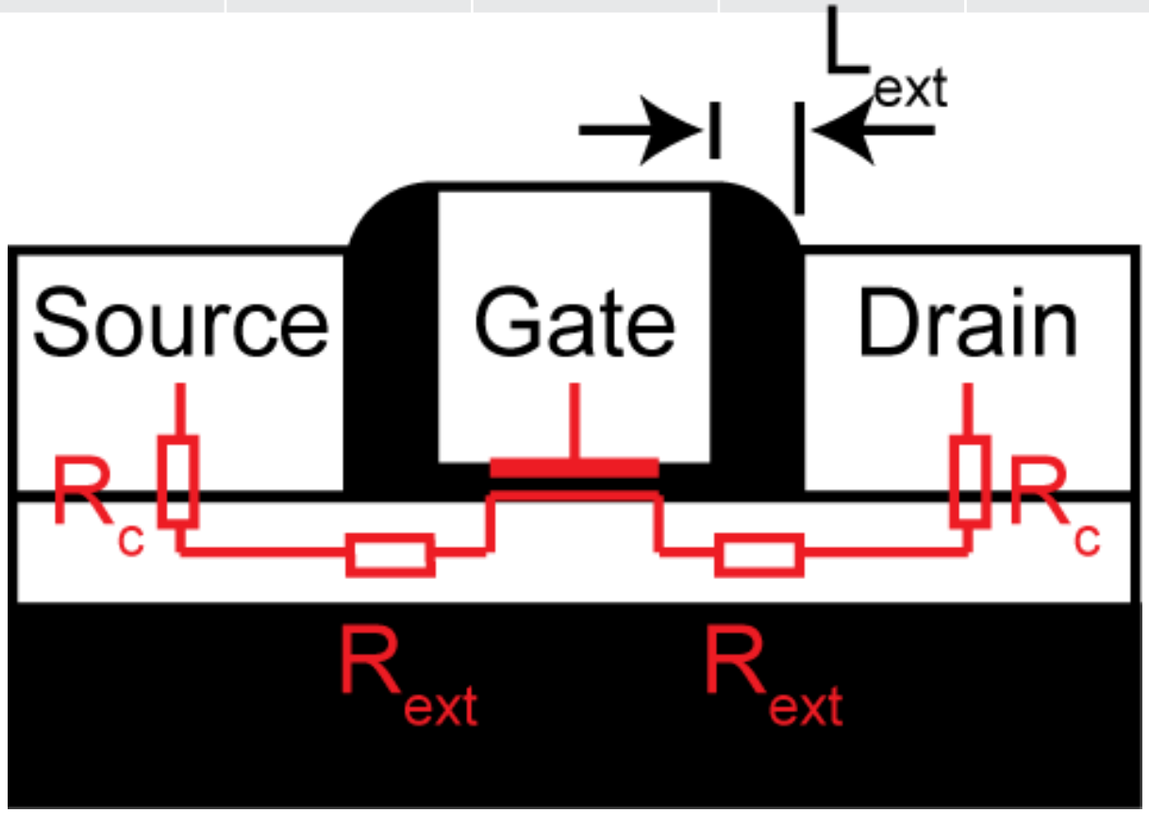


R. Oxland et al., IEEE EDL 33(4), 2012

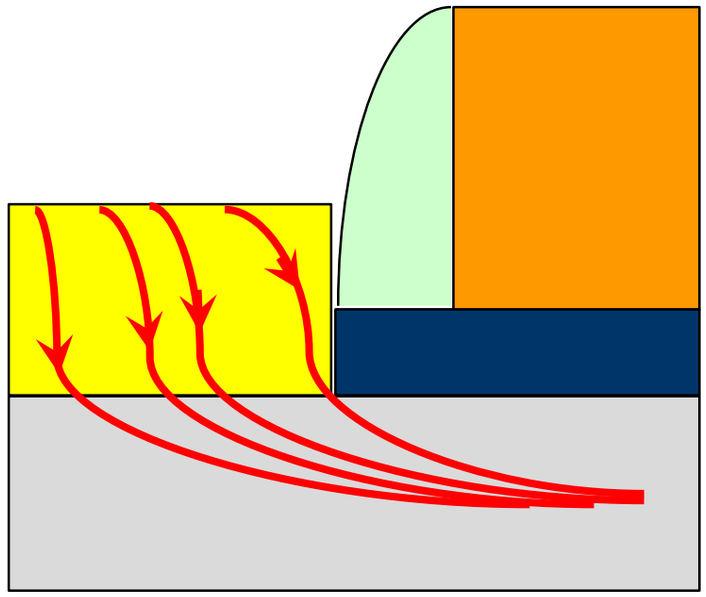
NiInAs S/D formation metal-NiInAs contact resistivity as low as 0.27 Ω.μm².

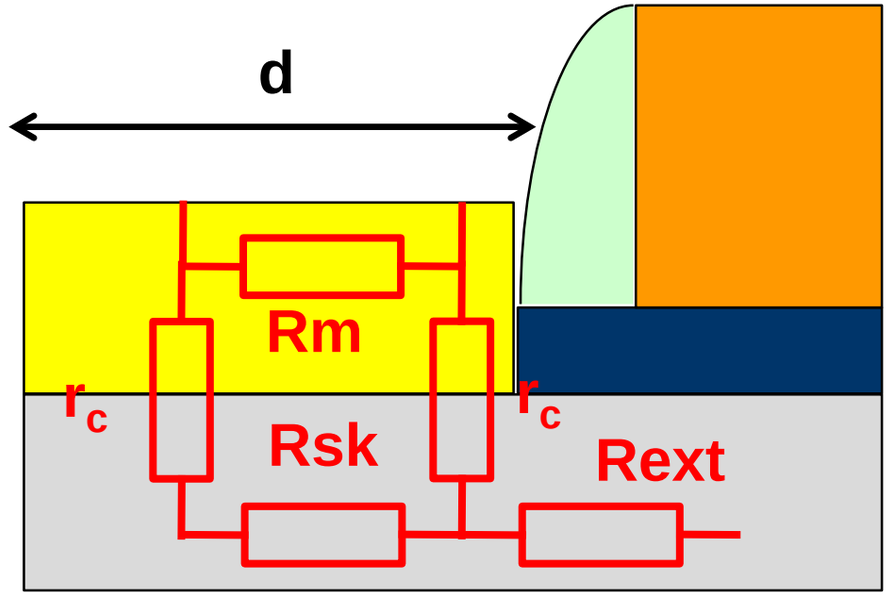
Source/drain contacts have to be optimised

Year	2011	2015	2018	2019	2020	2024
Gate Pitch (nm)	75	42	30	27	24	15
Physical gate length (nm)	24	17	13	12	11	7
Source/drain contact (nm)	21	10	6	5	5	2
Rsd (Ωμm)	160	140	130	120	120	110



So how does this impact device solutions





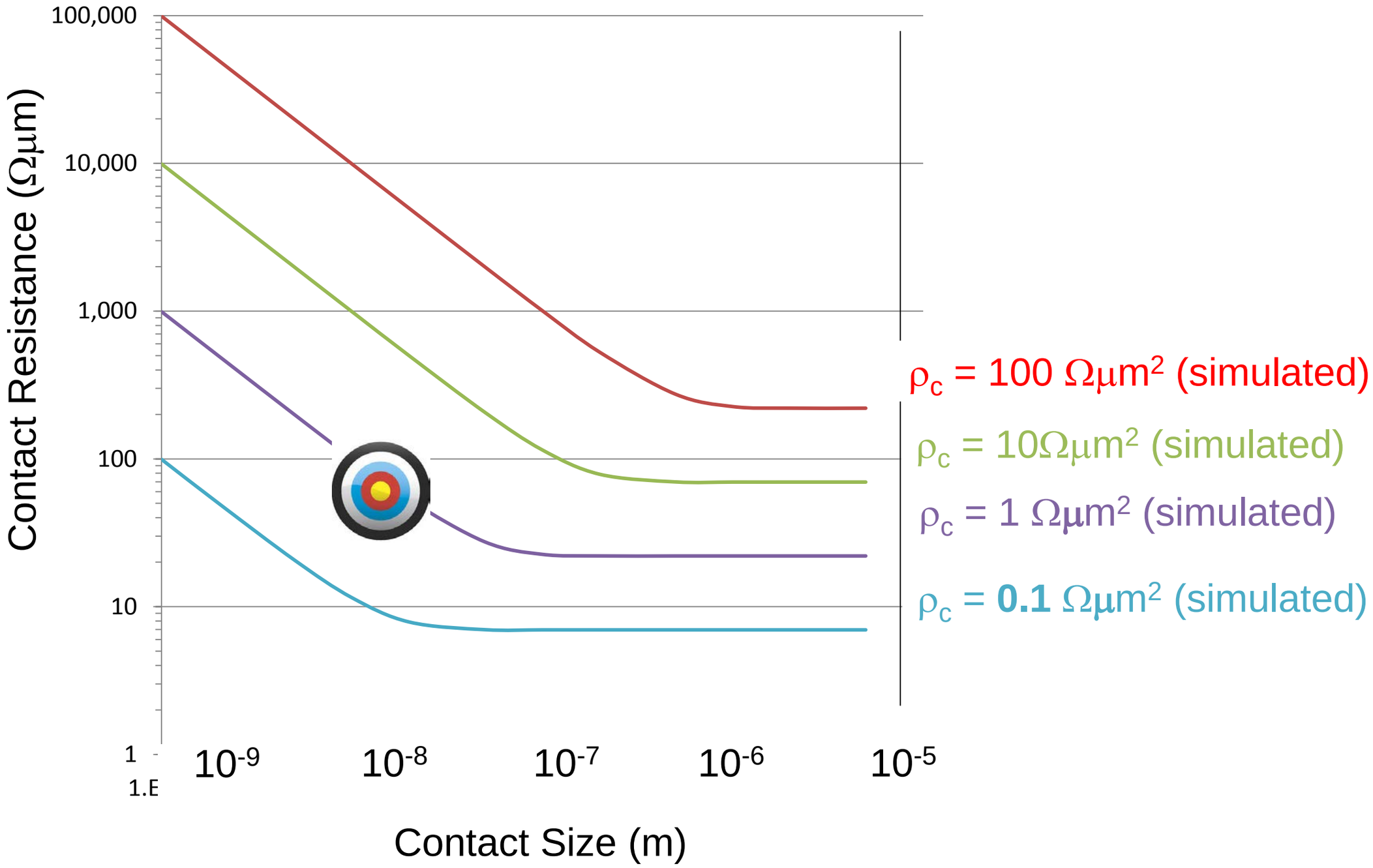
A distributed transmission line problem

If contact size d is less than "preferred" transfer length, L_T, contact resistance R_c increases dramatically

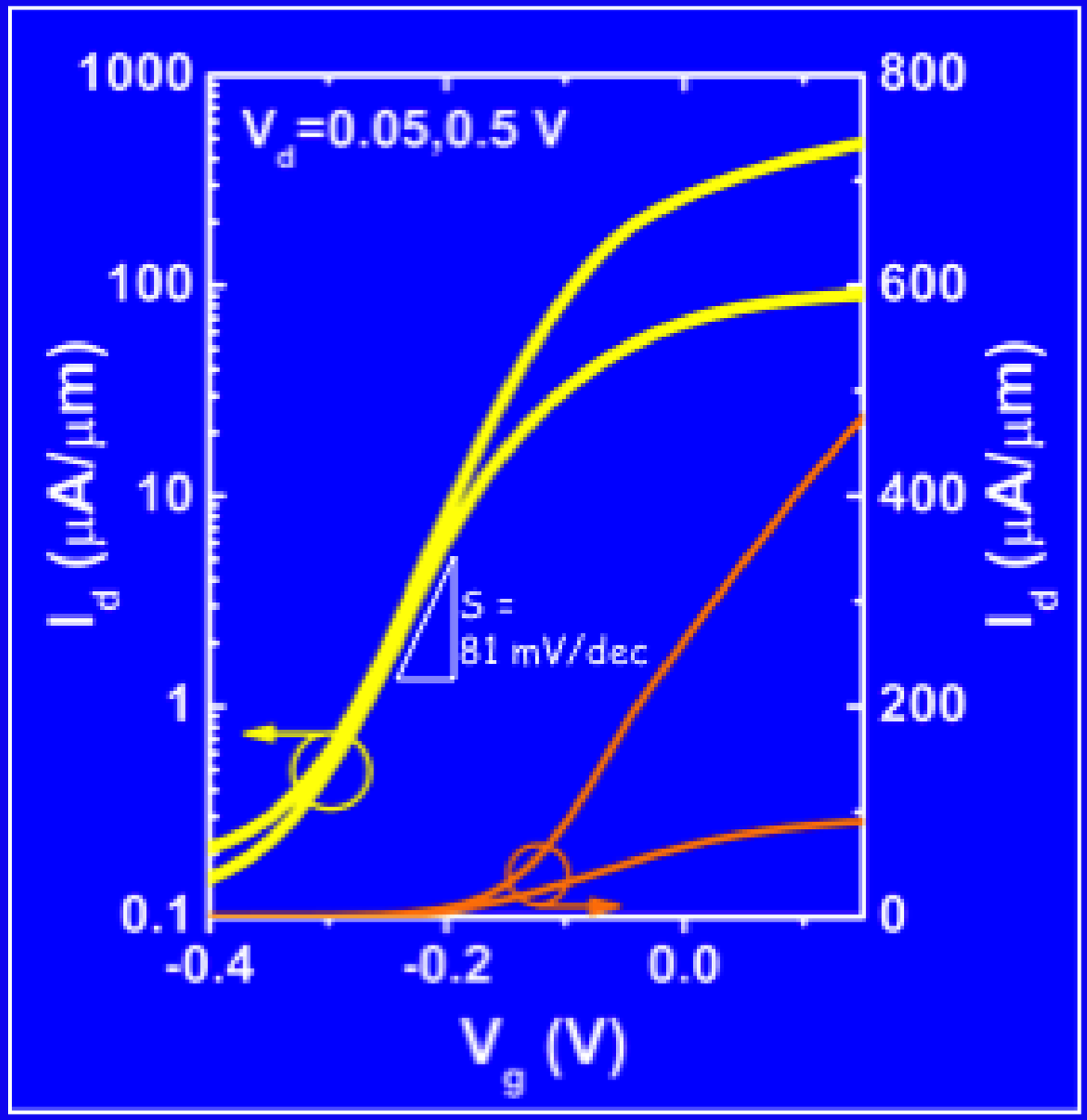
$$R_c = \frac{R_{sk} L_T}{W} \coth\left(\frac{d}{L_T}\right)$$

Berger Proc ISSCC, p160, 1969

Access resistance significant for sub-20 nm

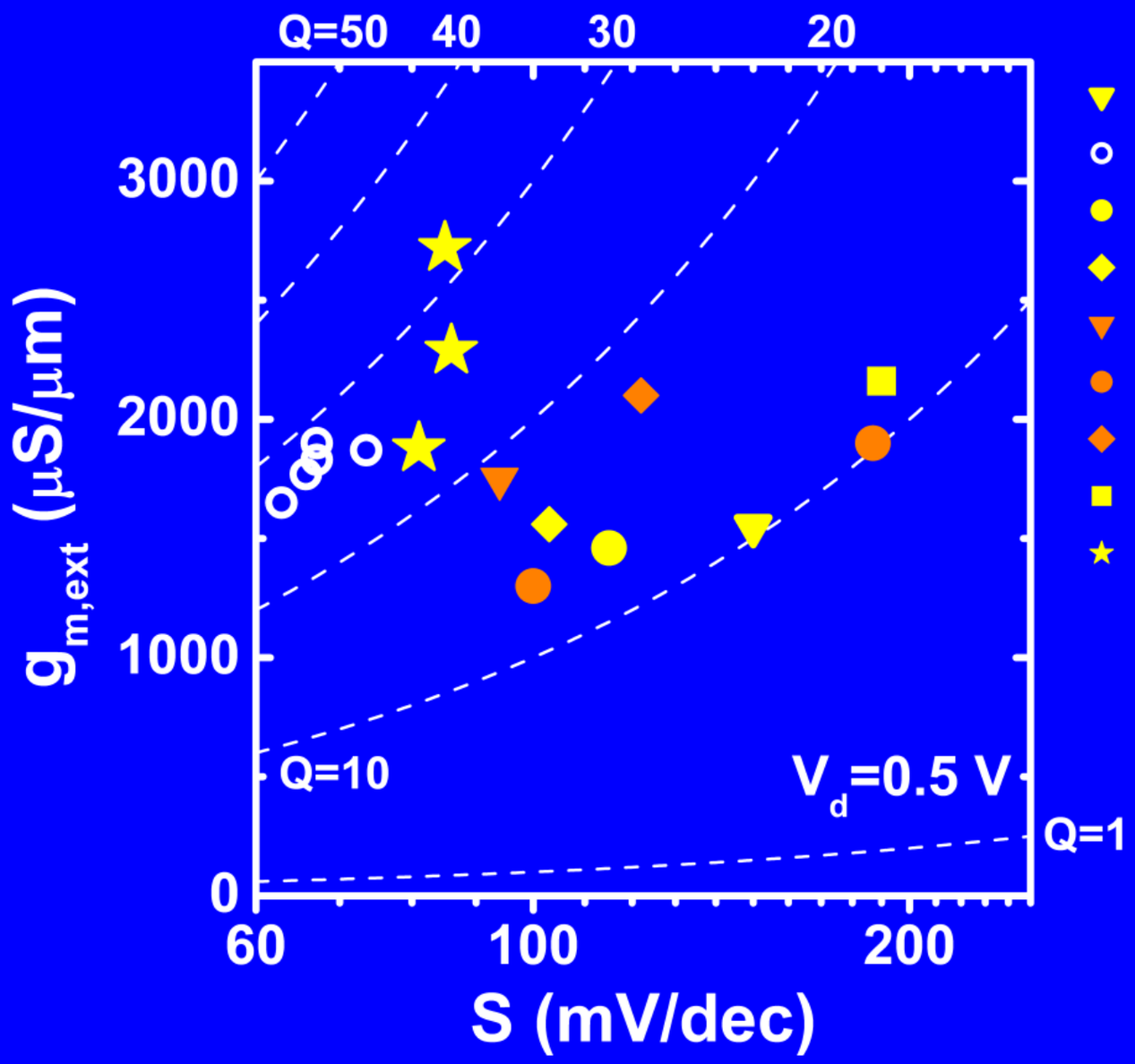


Sub-threshold swing – 81 mV/dec



The device I_d-V_g shows the high quality of the HK/InAs interface.

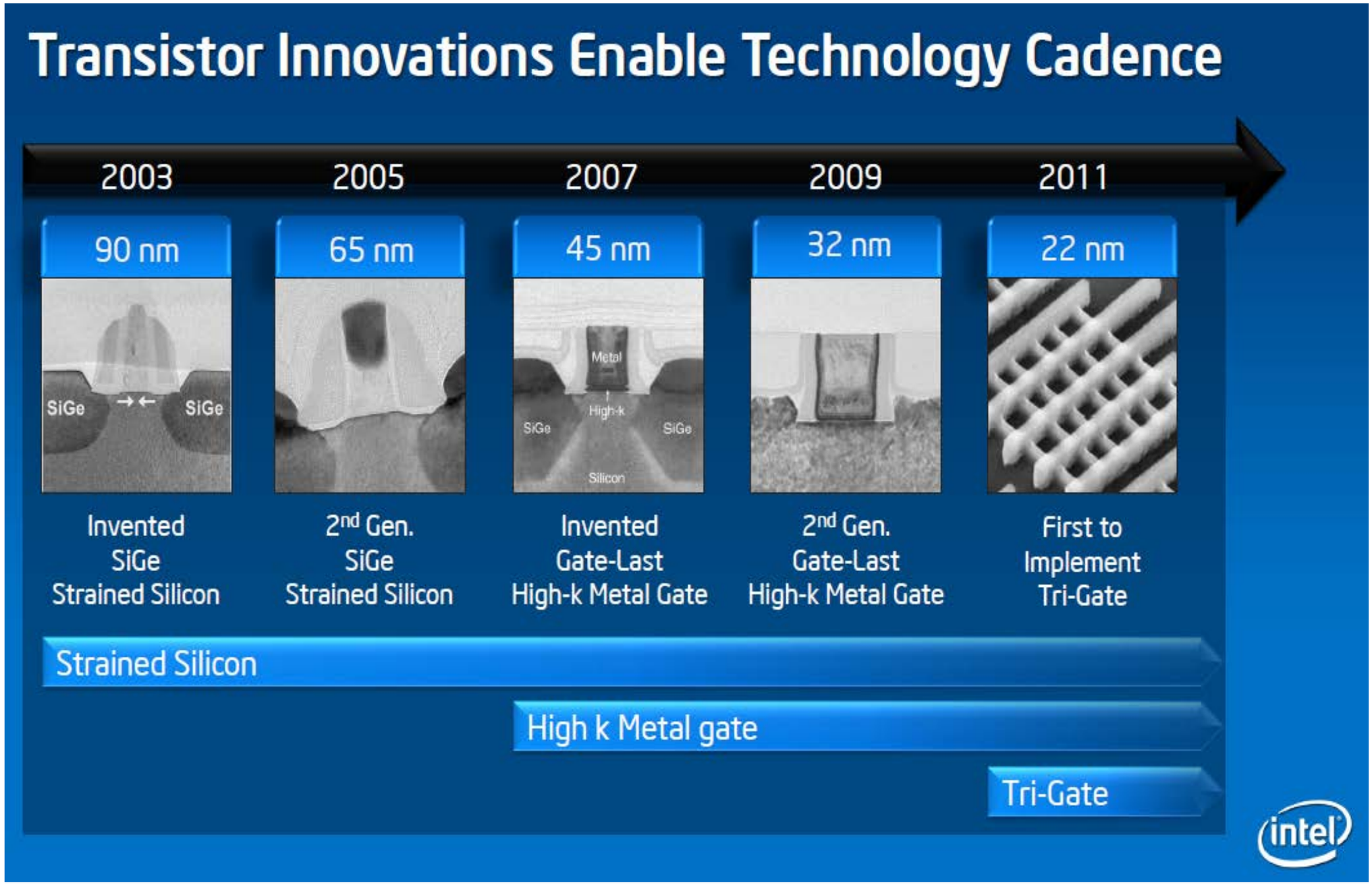
Planar III-V NFET Q = g_m/S benchmark.
Record Q = 33 for L_g = 130 nm



- [1] InAs XOI MOSFET
- [2] Inserted-InAs pHEMT
- [3] Inserted-InAs XOI MOSFET
- [4] Inserted-InAs MOS-HEMT
- [14] InGaAs MOS-HEMT
- [15] InGaAs MOSFET
- [16] InGaAs MOS-HEMT
- [17] Inserted-InAs MOSFET
- ★ This work (InAs MOSFET)

[1] H. Ko et al., Nature 468, p. 286 (2010)
[2] D.-H. Kim and J.A. del Alamo, IEDM 2008
[3] S.H. Kim et al., VLSI 2013
[4] T.-W. Kim et al., IEDM 2012
[14] M. Radosavljevic et al., IEDM 2009
[15] M. Egard et al., IEDM 2011
[16] D.-H. Kim et al., IEDM 2012
[17] S. Lee et al., VLSI 2013
This work

The future is non-planar……..

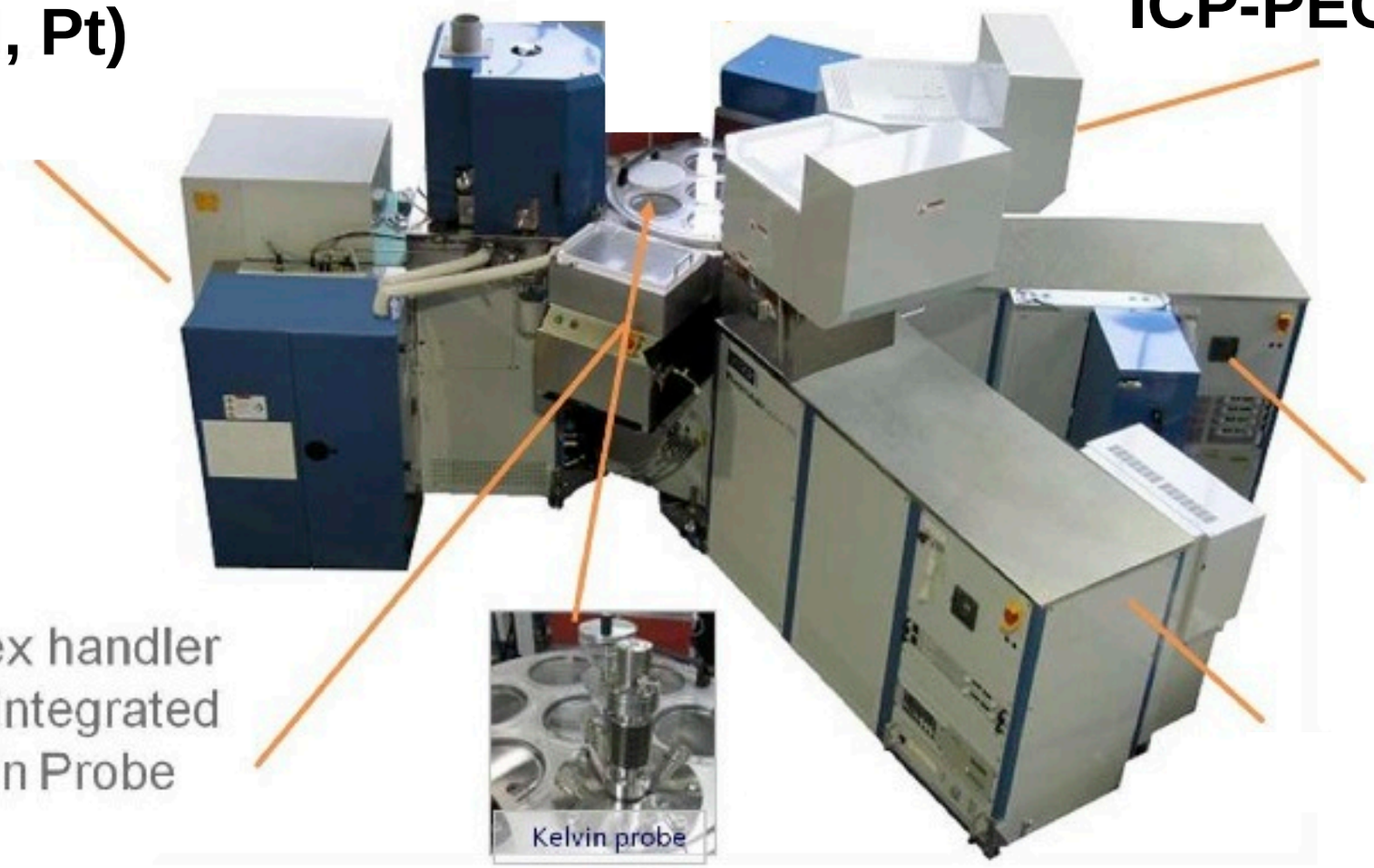


Recently Commissioned Equipment

- **EPSRC Capital for Great Technologies: Capability to Improve the Energy Efficiency of Electronic & Optoelectronic Devices**

ALD
(Al_2O_3, HfO_2, ZrO_2, TiN, TaN, Pt)

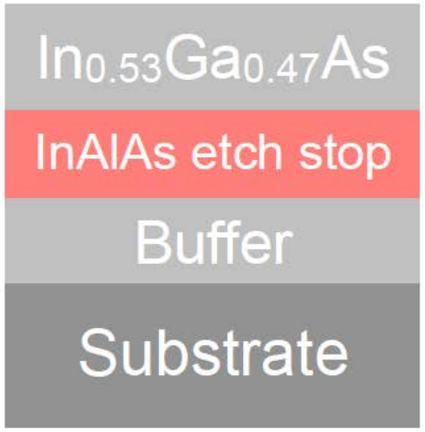
ICP-PECVD (Si_xN_y)



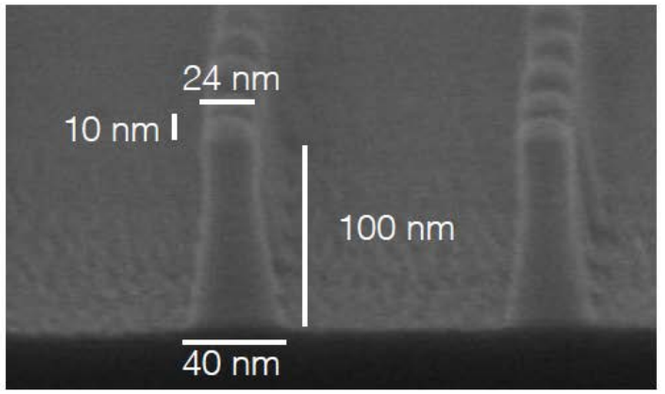
ICP-RIE etch (Cl_2, BCl_3, $SiCl_4$, HBr, etc....)

All 200 mm tools

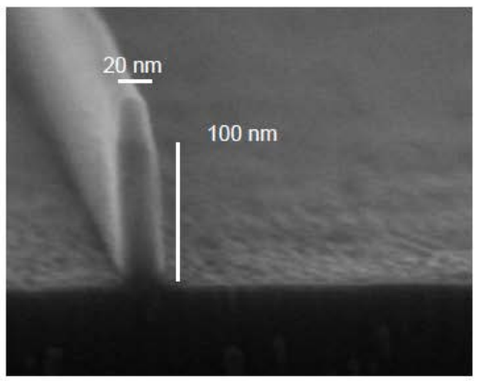
III-V finfets and nanowires



Epitaxial Layer structure

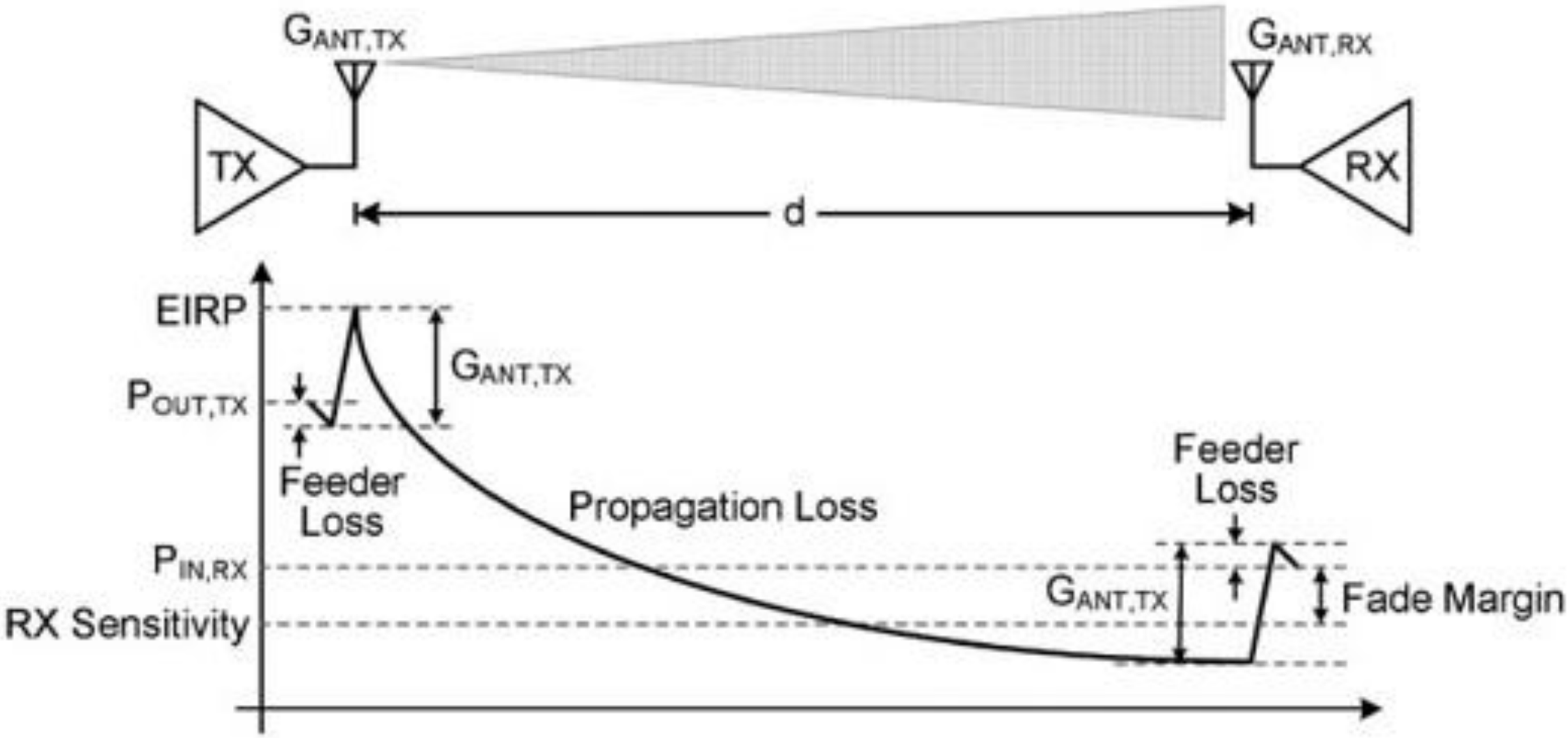


Etched nanowire without overetch

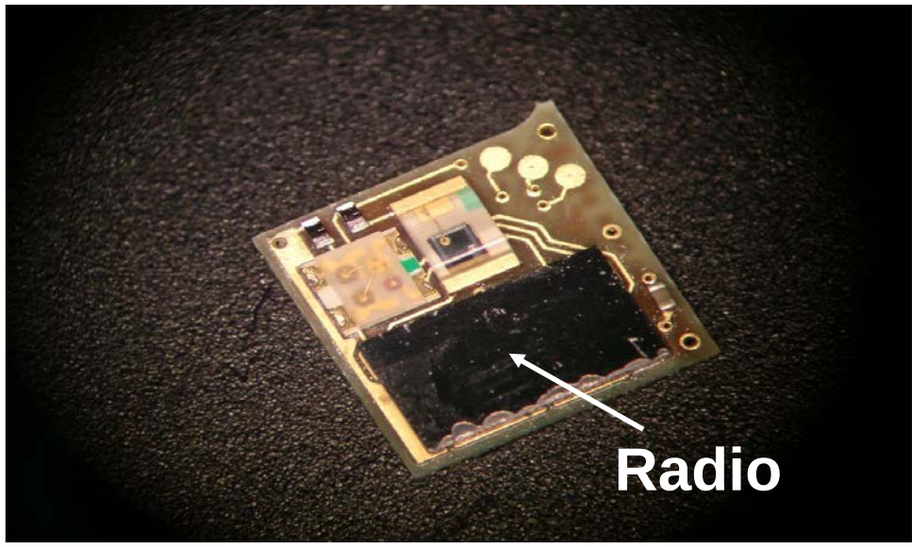


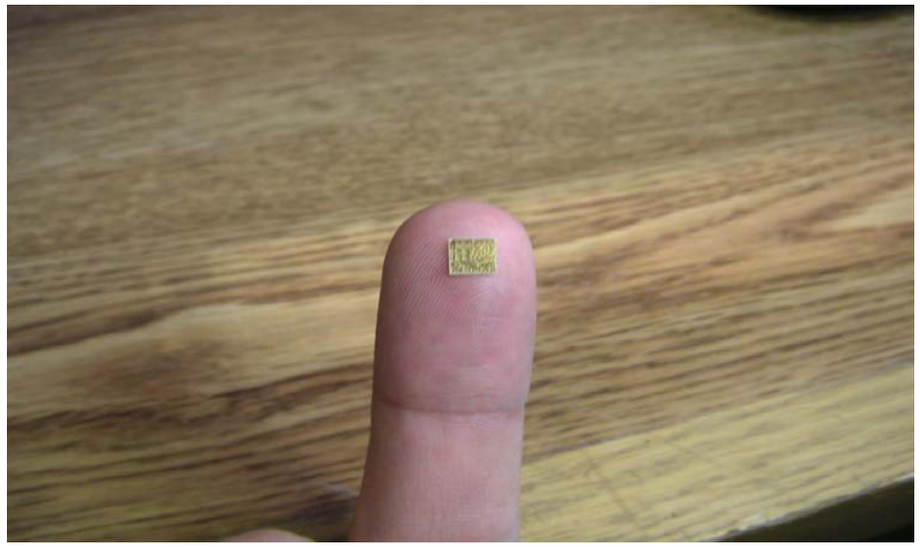
Etched fin with low bias over etch

Communicating the data



Wireless Communication

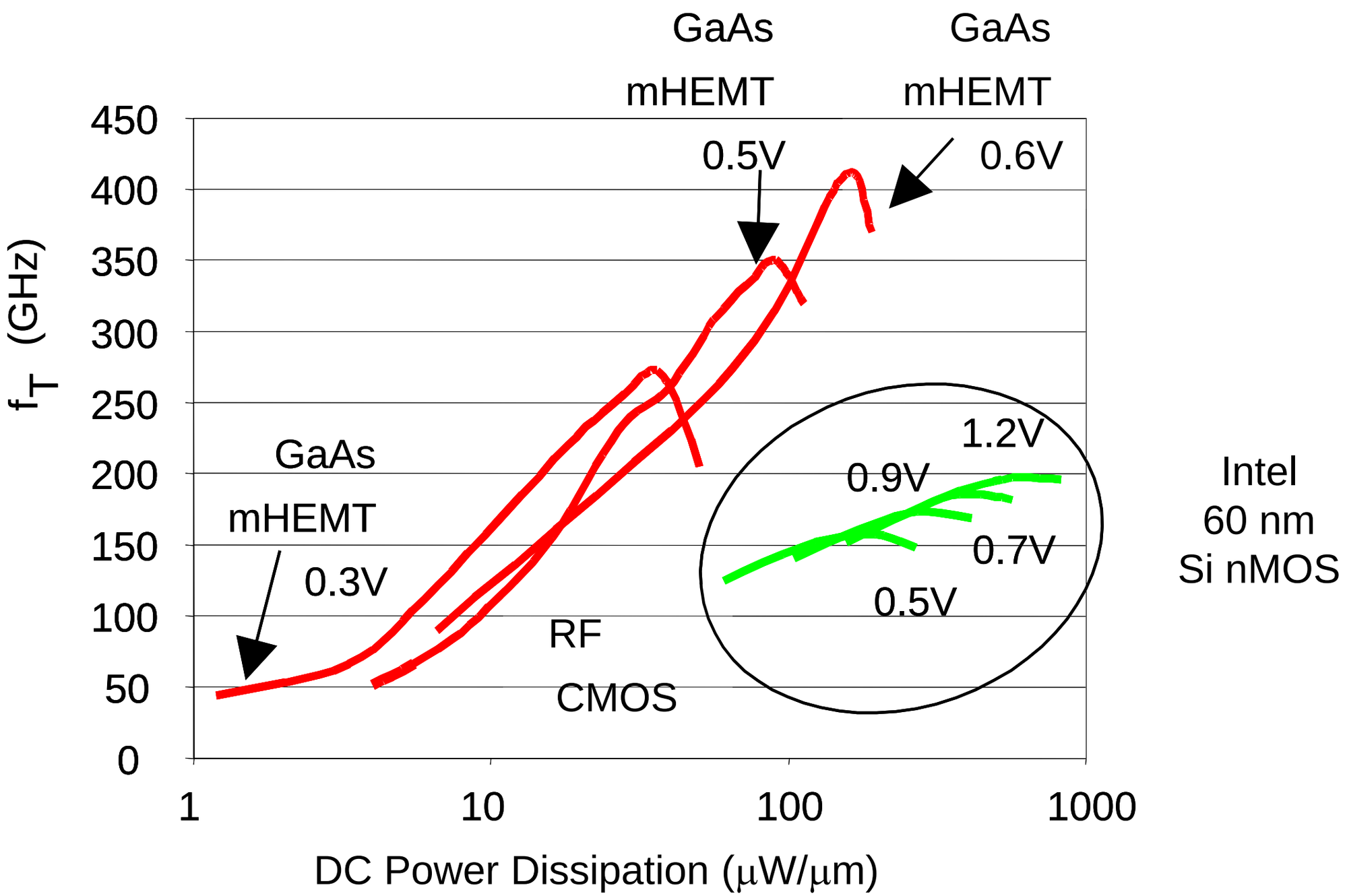




Key Radio Challenges

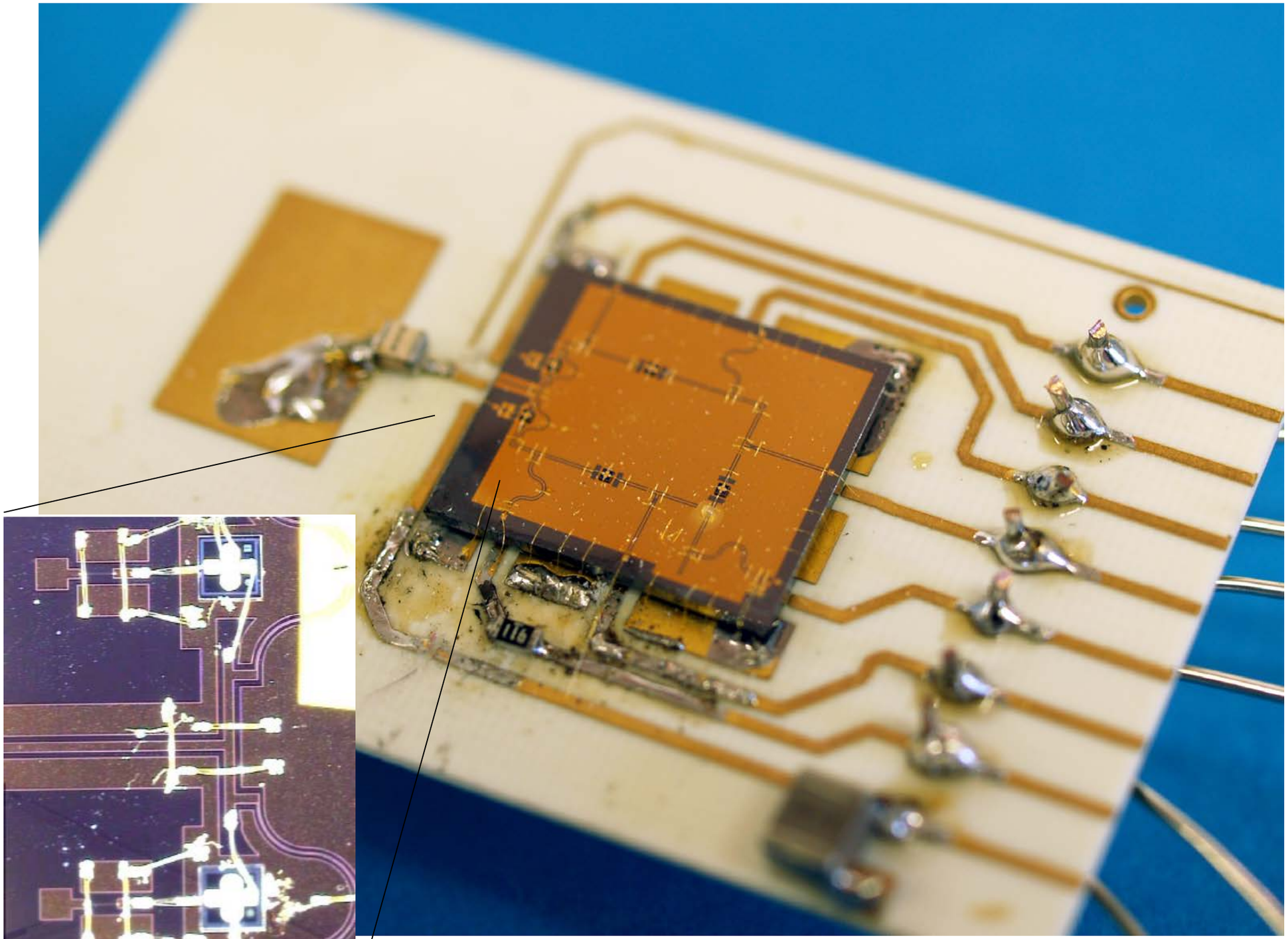
Low Power =>	**Reduce Operating Frequency**
	Better Power Added Efficiency,
	Reduced Noise
	Path Loss
Small Area =>	**Increase Operating Frequency**
	MMIC Chip and Antenna Size
High Data Rates =>	**Increase Operating Frequency**

III-V TransistorsRF Characteristics

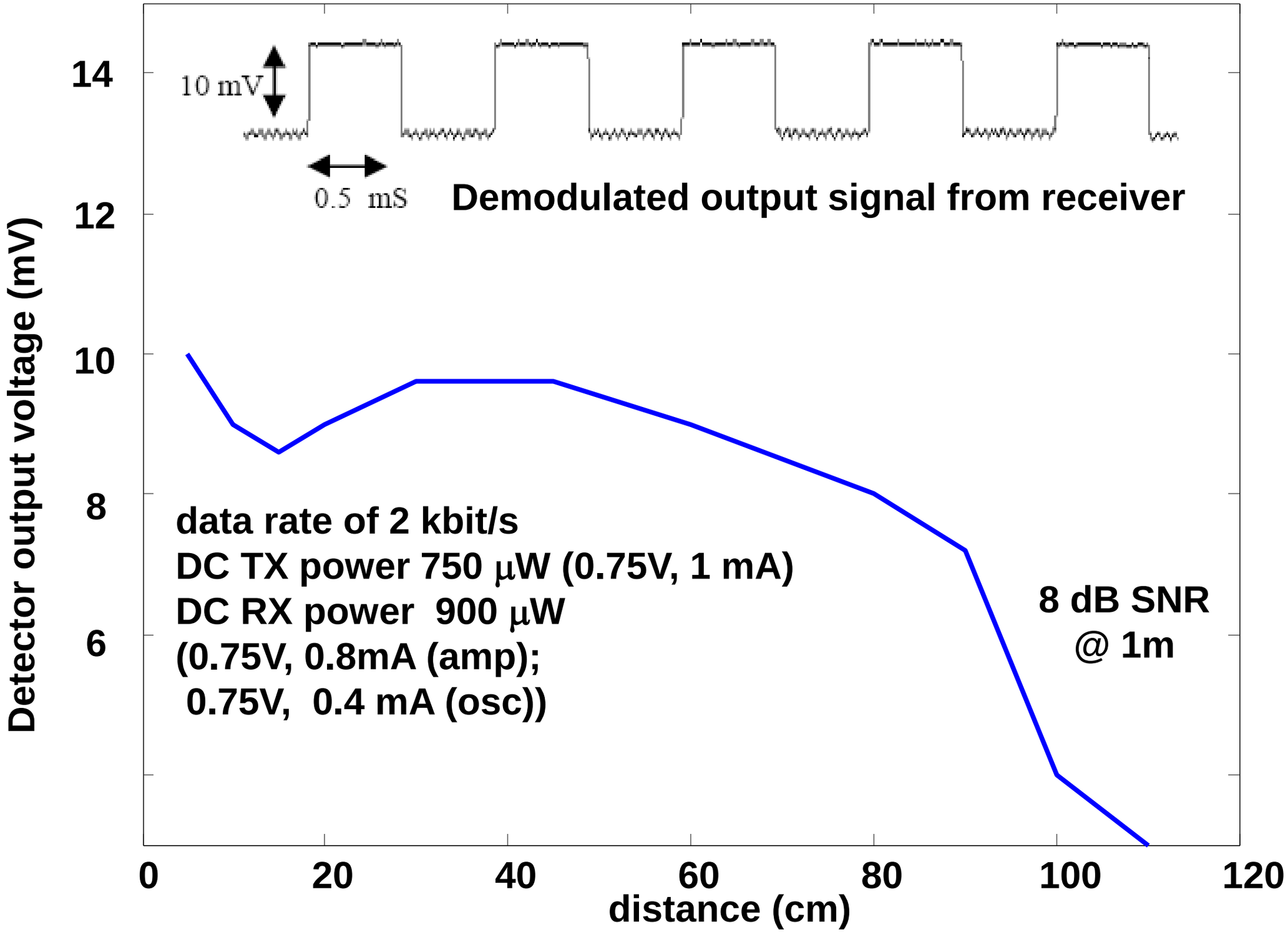


University of Glasgow

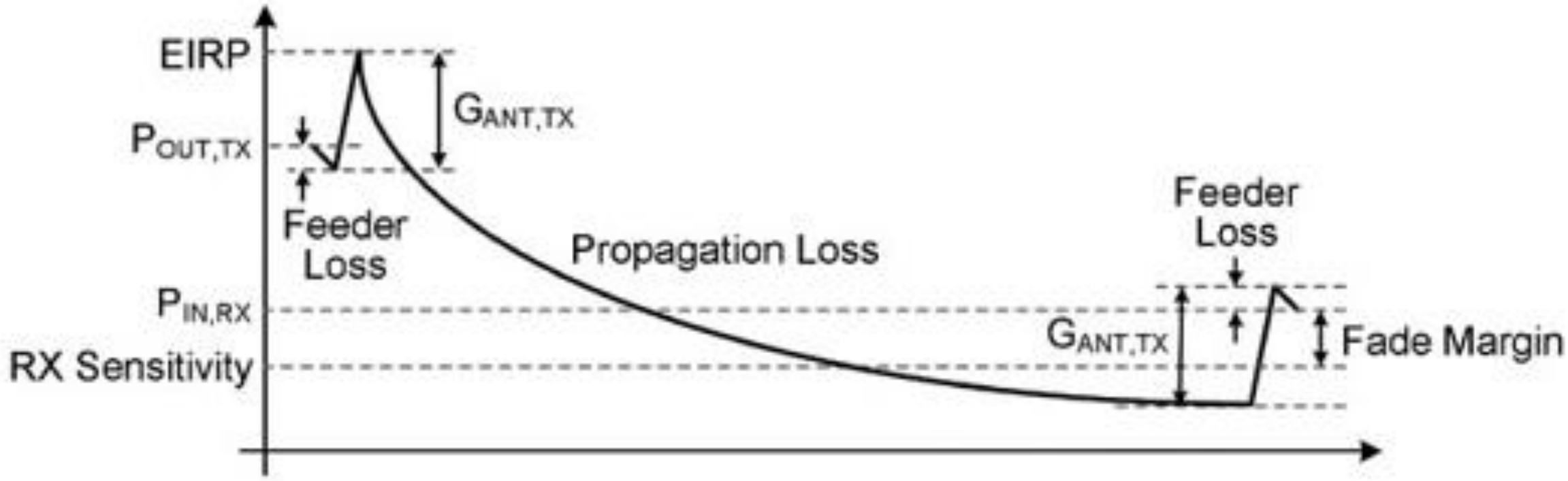
Low power circuit demonstrator



Low power circuit demonstrator



60 GHz indoor comms link budget



Frequency band (GHz)	57–66		
Link distance (m)	1/10		
FSPL (dB)	68/88		
Atmospheric loss (dB/km)	12 (sea level)		
Channel BW (GHz)	1.76		
TX/RX G_{ANT} (dBi)	5		
Feeder and implementation losses (dB)	5		
Modulation	64-QAM	16-QAM	QPSK
RX sensitivity at 10^{-6} BER (dBm)	−44.5	−50.5	−57.5
TX back-off (dB)	7.6	6.5	3.9
PA output power (dBm)	15		
Fade margin (dB) ($N_{TX/RX} = 16$)	24.9/4.8	32.0/11.9	41.6/21.5

15 dBm = 32 mW

Observations

Whatever the application, device solution, materials choice etc

- **Interfaces between materials is vital**
- **Low resistance contacts within and to the device are key**

The ICT System needs to be considered holistically

Switching losses in power electronics can be reduced ~2x

- **access resistance**
- **improved efficiency passive components**

Low power logic may give ~2x

- **reduced supply voltage**

High data rate wireless radio comms is a challenge

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