ICT-ENERGY LETTERS

Energy saving for logic switches operating at extreme low voltage conditions

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***Abstract*—In modern computers information is processed through binary switches, usually realized with transistors. These binary switches represent a paradigmatic example of "small scale physical systems" employed in the processing of information. In the last forty years the semiconductor industry has been driven by its ability to scale down the size of the CMOS devices, to increase computing capability and reducing the power dissipated in heat. Thus we assisted to a continuous reduction in the supply voltage and electrical noise induced errors became an important issue to take into account for the performance of the device. Here we propose a study of the relationship between the energy required by an advanced ultra low power logic gate and the associated error rate at different operating frequencies when the device is powered at very low voltage, lower than the minimum specified in the datasheet.**

I. INTRODUCTION

As a matter of fact, the energy issue is at the moment one of the major limitation in the development of both small autonomous wireless sensor nodes and large scale supercomputers. In the former case, computing devices are intended to be small (micro-nano scales) and self powered through some energy harvesting techniques [1-2]. Recently it has been suggested that the energy efficiency of the bit resetting operation can be improved allowing a finite error probability during operation [3, 5]. In this work a NAND gate has been tested to evaluate its performances at variable bit rate when its supply voltage is decreased below the minimum voltage specified by the producer. In this way it has been possible to identify the minimum supply voltage before error rate rises up to a non negligible limit. Reducing the supply voltage has an impact on the total power dissipation, but it is important to understand the quantitative correlation between the power saving and the error rate when the device is under-powered. It has been also investigated the behavior of the error generation trying to find if it can be predicted or not.

II. ENERGY DISSIPATION IN LOGIC SWITCHES

In the last forty years the progress of the semiconductor industry has been driven by its ability to cost effectively scale down the size of the CMOS-FET [6] switches while increasing their density. This has been accompanied by a continuing increase in energy consumption and heat generation up to a point where the power dissipated in heat during computation has become a serious limitation [7, 8]. It has been shown that information processing is intimately related to energy management ("information is physical")[4]. The ultimate limit on the minimum energy per switch resetting is set at $K_BT\ ln2$ (approximately 10^{-21} J at room temperature) [4, 9] while there is no fundamental limit associated with the switching operation per sè [3]. This limit is known to be the Shannon-von Neumann-Landauer (SNL) limit. Two components determine the power consumption in a CMOS circuit: static power consumption and dynamic power consumption [10]. The first is proportional to the current flowing into the device as a consequence of leakages; the second one is related to the current required during switching. CMOS devices have very low static power consumption because parasitic diodes are reverse biased and only their leakage currents contribute to static power consumption. The leakage current (I_{lkg}) of the diode is described by the following equation (1)

$$I_{lkg} = I_S\left(e^{\frac{qV}{kT}} - 1\right) \quad (1)$$

Where:

I_S = reverse saturation current (A)
V = diode voltage (V)
k = Boltzmann's constant (1.38×10^{-23} J/K)
q = electronic charge (1.602×10^{-19} C)
T = temperature (K)

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption PS can be obtained as:

$$P_S = \sum(\text{leakage current}) \cdot (\text{supply voltage}) \quad (2)$$

Dynamic power consumption is due to the current that flows only when the transistors are switching from one logic state to another. This is a result of the current required to charge the internal nodes (switching current) plus the through current (current that flows from the supply voltage VCC to GND when the p-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance. If we consider the energy required to drive an inverter's output high and low, this is the same of loading and discharging a capacitor C_L through a resistor R_L. The energy stored and dissipated in the resistor and capacitor is given by the equation (3) and (4) respectively:

$$E_{R_L} = \int_0^\infty \frac{V_{R_L}^2(t)}{R_L} dt = \frac{V}{R_L}\int_0^\infty \left[e^{\left(-\frac{t}{R_L C_L}\right)}\right]^2 dt = \frac{C_L V^2}{2} \quad (3)$$

$$E_{C_L} = \frac{C_L V^2}{2} \quad (4)$$

Considering NSW working at the frequency fI, the energy dissipate can be obtained by the equation (5).

$$P_T = \alpha \cdot (E_{R_L} + E_{C_L}) \cdot f_I \cdot N_{SW} = \alpha \cdot C_{pd} \cdot {V_{CC}}^2 \cdot f_I \cdot N_{SW} \quad (5)$$

where:

P_T = transient power consumption (W)

α = activity factor, α=1 for a square wave switching and α<0.5 in typical digital circuits

C_{pd} = dynamic power-dissipation capacitance (F)

V_{CC} = supply voltage (V)

f_I = input signal frequency (Hz)

N_{SW} = number of bits switching

III. THE EXPERIMENTAL SETUP

An experiment has been performed to obtain a relationship between the bit error-rate and the power consumed by a logic device, a SN74AUP1G00 [11] two inputs single NAND gate from Texas Instruments. The experimental setup is composed by a stable voltage supply, a variable voltage supply, a signal generator, a digital comparator, a temperature sensor, some current to voltage converters and an asynchronous counter. The block diagram of the experimental setup is depicted in Fig. 1.

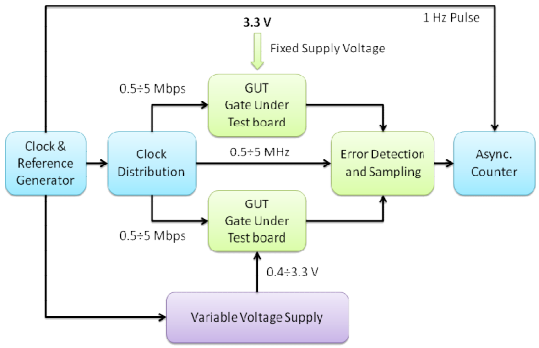

Fig. 1 Block diagram of the system designed for the evaluation of the error rate.

Two of GUT boards (GUT Gate Under Test board) are used in parallel. In the first one, the NAND gate is always powered at the nominal voltage of 3.3 V: in this way no errors are expected during its working time. In the other board, instead, the NAND gate is powered from a variable voltage power supply. An EX-OR is used as bit comparator to detect errors. At its input the output signals of the GUT boards are presented. When the two inputs are not equal, the output of the comparator goes to the logic level "1". This is the error detection condition required during this experiment.

IV. MEASUREMENTS AND RESULTS

Several measurements have been performed and the overall results are presented in Fig. 2 where the correlation among the dynamic current, the error rate and the voltage gap between the two logic states at different bit rate and variable supply voltage (0.4 V to 8.8 V). From these measurements is possible to obtain an estimation (equation (6)) of the overall (internal and external load capacitance) power dissipation capacitance C_e: it is in good agreement with the predictions.

$$C_e = \frac{I_{CC}}{V_{CC} \cdot f_o} \approx 16\,pF \tag{6}$$

The plots of Fig. 2 show the dynamic currents, the error rates and the voltage gaps respectively at different bit rates and when the supply voltage ranges between 0.4 V and 0.8 V. Considering the dynamic current of the gate at different bit rates as function of the supply voltage, there are points where the slope of the curves changes. These points are few tens of mV higher than the point where the error rates rise and can be interpolated by and exponential curve as function of the supply voltage (equation (7)).

$$I_c = 0.08774e^{(10.64 \cdot V_{CC})} \tag{7}$$

The error rates curves as function of the bit rate and the supply voltage can be approximated by an *erfc* function defined as in the (8). All these error functions are parallel to each other and they appear to be only translated: it is possible to obtain the translation coefficients values V_{Tr}: they are linearly dependant by the bit rate BR (9):

$$erfc(V_{CC}) = \frac{2}{\sqrt{\pi}} \int_{V_{CC}}^{\infty} e^{-t^2}\,dt \tag{8}$$

$$V_{Tr} = 0.0315 \cdot B_R + 0.428 \tag{9}$$

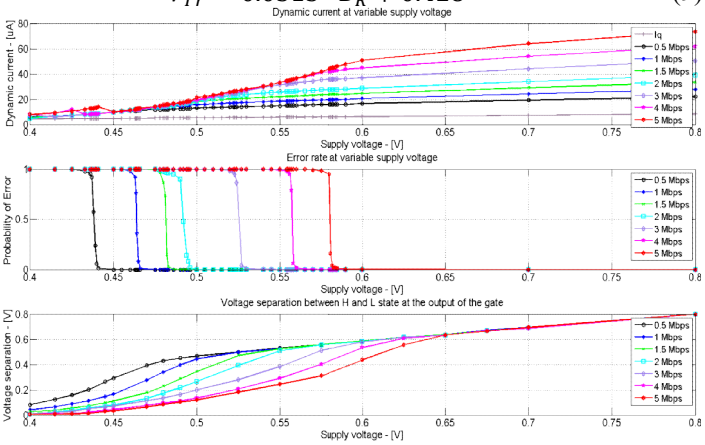

Fig. 2 Detail of the results of the measurements of the dynamic current, of the error rate and of the voltage gap between the high and low level of the output of the NAND gate.

It is possible to propose a phenomenological model for $I_{CC}(V_{CC})$ and $Pe(V_{CC})$. It can be noted the absence of a step-like behavior for $V_{CC} = V_{T2}$, i.e.: $Pe(V_{CC}) = 0$ for $V_{CC} > V_{T2}$ and $Pe(V_{CC}) = 1$ for $V_{CC} < V_{T2}$. This seems to indicate the role played by the voltage/threshold fluctuations and the device failure appears to be a stochastic phenomenon other than a deterministic event.

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