Single Electron Devices and Circuits

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The MOSFET: workhorse of the ME industry

Microprocessor

5.5 billion transistors
18-core Xeon Haswell-EP

Flash memory

256 billion transistors
weighting 0.5 g
Downscaling drove progress

Improving computers for 50 years

f,V scaling stopped

Moore’s Law (any time now …)

Power Wall

Multicore era
Downscaling will not work forever

• Loss of control over the channel electrostatics – Short Channel effects

Ferain et al, Nature 479 310

• Static vs Dynamic Power

E. Pop, 2010
Gate-based RF readout for QIP

Single Electronics
Coulomb Blockade

SET Conditions

\[ R_T > 25.6k\Omega \]
\[ E_c = \frac{e^2}{C_\Sigma} > k_B T \]

Energy of the system with N electron

\[
U(N, V_g) = \int_0^{-Ne} V(Q)dQ = \frac{N^2 e^2}{2C_\Sigma} - \frac{NeC_gV_g}{C_\Sigma}
\]

Energy difference between N and N-1 electrons

\[
\mu(N, V_g) = U(N, V_g) - U(N - 1, V_g) = \frac{e^2}{C_\Sigma} (N - 1/2) - \frac{eC_gV_g}{C_\Sigma}
\]
Single-Electron Functionality

Coulomb Blockade

\[ R_T > 25.6k\Omega \]

\[ E_C = \frac{e^2}{C_\Sigma} > k_BT \]

SET Conditions

SET

\[ \text{SET Conditions} \]

\[ R_T > 25.6k\Omega \]

\[ E_C = \frac{e^2}{C_\Sigma} > k_BT \]
**Single-Electron Functionality**

**Coulomb Blockade**

**SET Conditions**

\[ R_T > 25.6k\Omega \]

\[ E_c = \frac{e^2}{C_\Sigma} > k_B T \]
Switching Characteristics - Subthreshold Slope

**MOSFET**

\[ SS = \ln(10) \frac{kT}{q} \left(1 + \frac{C_d}{C_{OX}}\right) > 60 \text{ mV/dec} \]

**Single Electron Transistor/Single Atom Transistor**

\[ SS_{SET} = 1.25 \cdot \ln(10) \frac{kT}{aq} > 75 \text{ mV/dec} \]

\[ SS_{SAT} = \ln(10) \frac{kT}{aq} > 60 \text{ mV/dec} \]
Why do we care about single-electron devices?

Exploit the non monotonic transfer characteristics of the devices
New Functionalities – Complex Logic at the Device Level

Devices Explored
- Single Electron Transistor (SET)
- Single Atom Transistor (SAT)
- Magnetic Single Electron Transistor (MSET)
Single-Electron Devices based on CMOS transistors
3D Fully-Depleted Silicon-on-insulator FET

- 300mm SOI wafers
- Gate stack
- Poly-Si
- Spacer
- BOX
- Si-Back Gate
- $t=9-11\,\text{nm}$

$w>10\,\text{nm}$  $L>10\,\text{nm}$
Great Transistors at Room Temperature

W7 (Spacer 5nm, Channel doping $5^{17}$) $W=10-15nm$

Good electrostatic control in Trigate Nanowires

$\text{DIBL} \sim 100 \text{ mV/V at } L_G=15\text{nm and } \text{SS}_{\text{SAT}} \sim 70\text{mV/dec at } L_G=15\text{nm}$

Comparable to the SoA optimized NWFET: DIBL=80mV/V for Lg=10nm
At Low Temperature is a Single Electron Transistor

DC @ 30mK \( w=10 \text{ nm} \) \( L=64 \text{ nm} \)

A. C. Betz et al.
App. Phys. Lett 104 043106

Single- Electron Transistor

- Confinement along the transport direction:
  - Nitride spacer,
  - Surface roughness
  - Remote charges at the gate stack
- Typical charging energies 20 meV \( - T =20K \)
- First electron \(~0.52\pm0.01 \text{ V} \) (Good reproducibility)
Or a Single Atom Transistor

Single Boron Transistor
- Charging energy 30-50 meV – T =30-50 K
- Random distribution of dopants
- Spin Filter

Van der Heijden et al. Nano Letters 14 1402 (2014)
And can even work at room temperature

SET working at room temperature
- Ω-gate transistor 3.4 nm diameter, 10 nm gate
- Charging energy 230 meV due to surface roughness
- Difficult to produce in large scale: ~10% CBO

Lavieville et al. Nano Letters 15 2958
3. SE Circuits and Architectures

![Circuit Diagram]

- **a)** Circuit with `OR` and `NAND`
- **b)** Circuit with `AND` and `NOR`
SET-FET hybrid circuits for amplification

- Typical SET current ~1nA
- Amplification by MOS: $10^6$
- Output Impedance 1k, output current 1 mA

Reconfigurable Logic using Magnetic Transistors

Ferromagnetic Gate Electrode: GaMnAs gate

Complementary Functionality

Reconfigurable Logic using Magnetic Transistors

Magnetic SETs Circuits

- N and P type on same device
- NAND to NOR reconfigurability done at single device level
- OR-NAND, AND-NOR done at circuit level
- Need to find large magnetic anisotropy material – CoPt ~ 60mV

Logic Circuits with Single Electron Devices

1-Bit Full Adder

• Using 1 SET + 1 SAT + 2 CMOS (vs 28 CMOS)
• Implement Logic at the hardware level- Ternary
• CMOS compatible
• SET decodes SAT to binary
• 2 CMOS provide concatenation for the carry

Mol et al. PNAS 108 13969
Dual Mode Architectures

Idea: Why not use both encodings at the same time on the same circuits

Binary encoding: “precise” version, full cost in computing and storage
Multivalued encoding: “approximate” version, reduced cost in computing and storage

Further: use both encodings in the same data word
a few digits (most significant) binary
the rest (least significant) multivalued

Sjalander et al. WAPCO 2016
Conclusion

1. Single Electronics:
   a. Single Electron Device present non-monotonic I-V characteristics that allow for implementation of complex operations at the device level.

2. Device:
   a. FD-SOI is suitable for single-electron device implementation up to room temperature
   b. SET reliable threshold voltage at low temperature but reproducibility problems at room temperature

3. Circuits and Architectures:
   a. Hybrid SET-FET circuits for permit large single-electron fanout
   b. Complex logic implementation at the device level reduces circuit complexity and power consumption
   c. Dual-mode architecture for approximate computing – Quaternary SE devices
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