Energy saving for logic switches operating at extreme low voltage conditions

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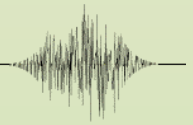
NiPS Laboratory
Noise in Physical Systems



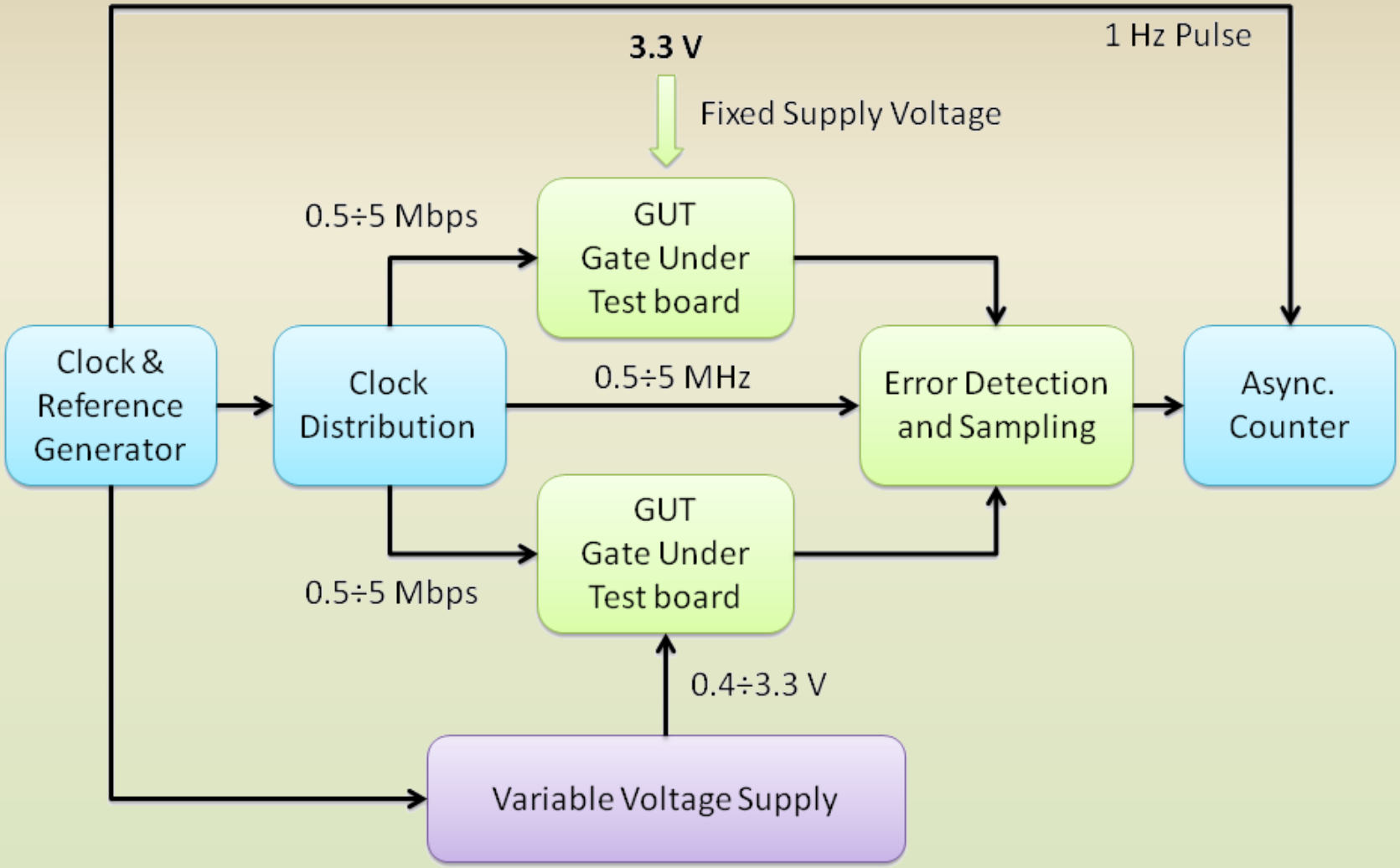
Outline

- Introduction
- Block diagram of the test system
- Measurement procedures
- Tests and Measurements
- Conclusions

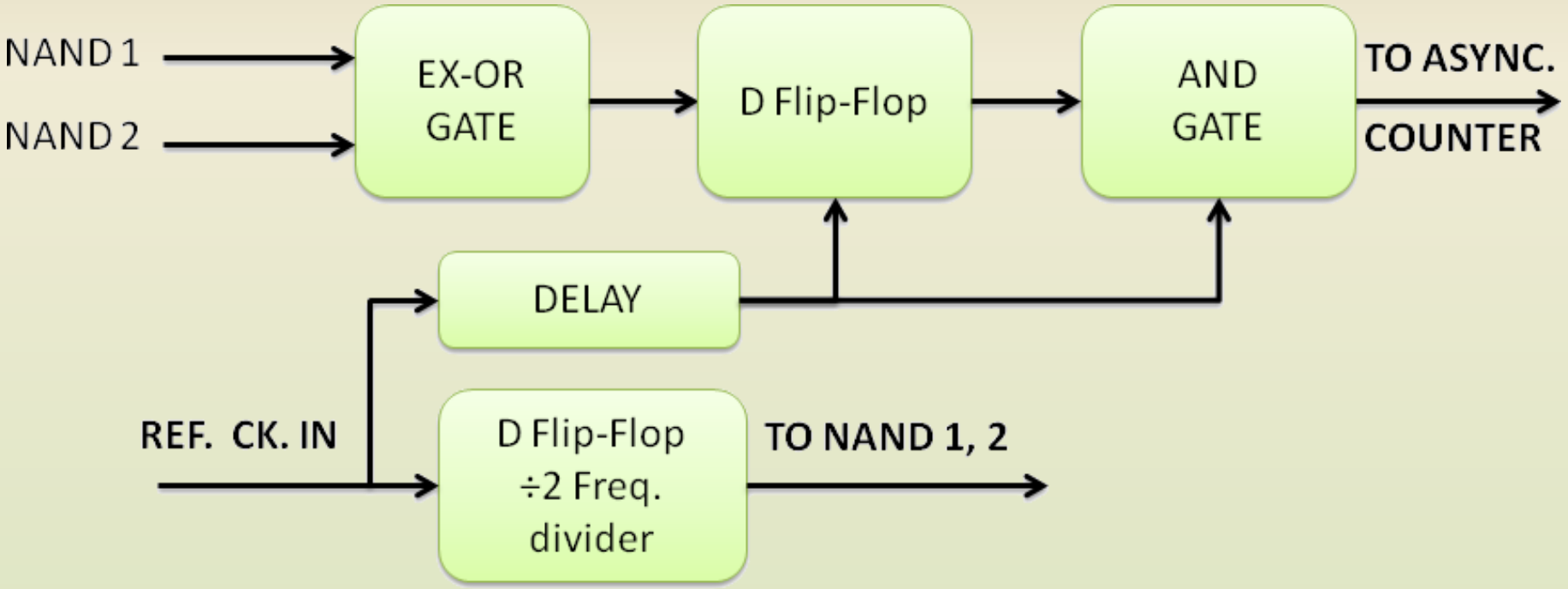
Introduction

- Which is the minimum energy of computing for a logic switch?
- Which is the minimum supply voltage for a logic switch before it stops working?
- What about the error rate in a logic switch?
- How much energy can be saved when accepting a given error rate?

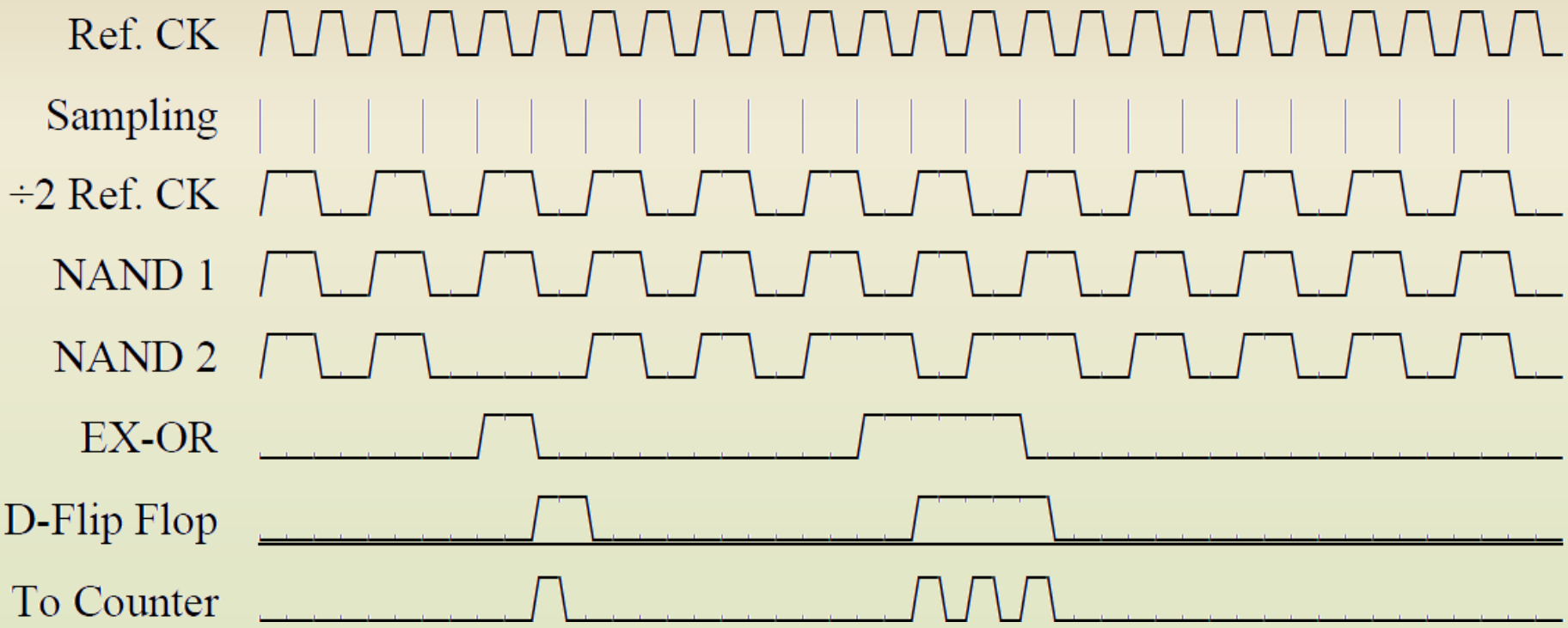
Block diagram of the test system



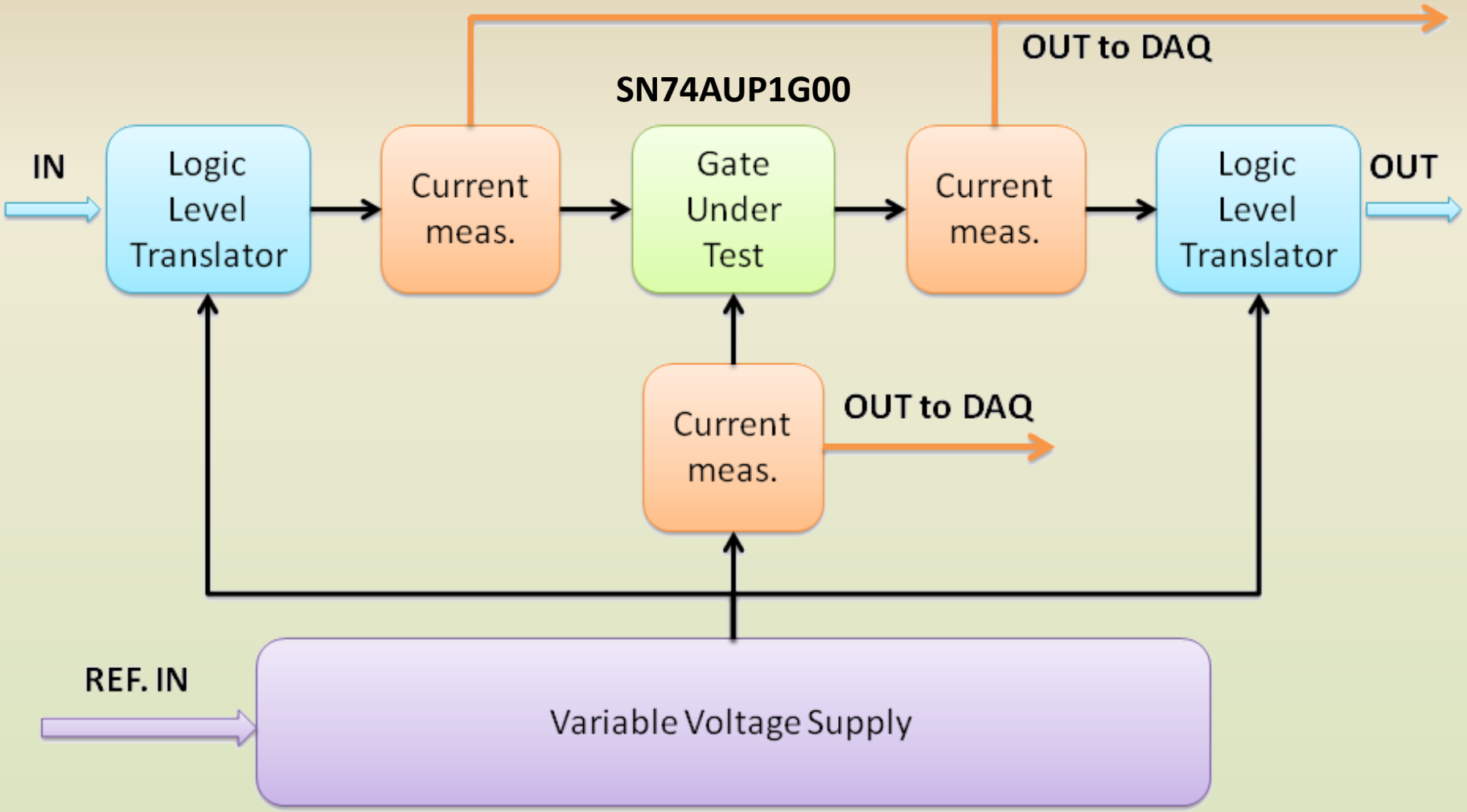
Error detection and clock management circuitry



Expected signals



Block diagram of the board for the Gate Under Test



Board for the Gate Under Test

SIGNAL CONDITIONING AND CURRENT MEASUREMENT BOARD

NAND
+
TEMPERATURE
SENSOR

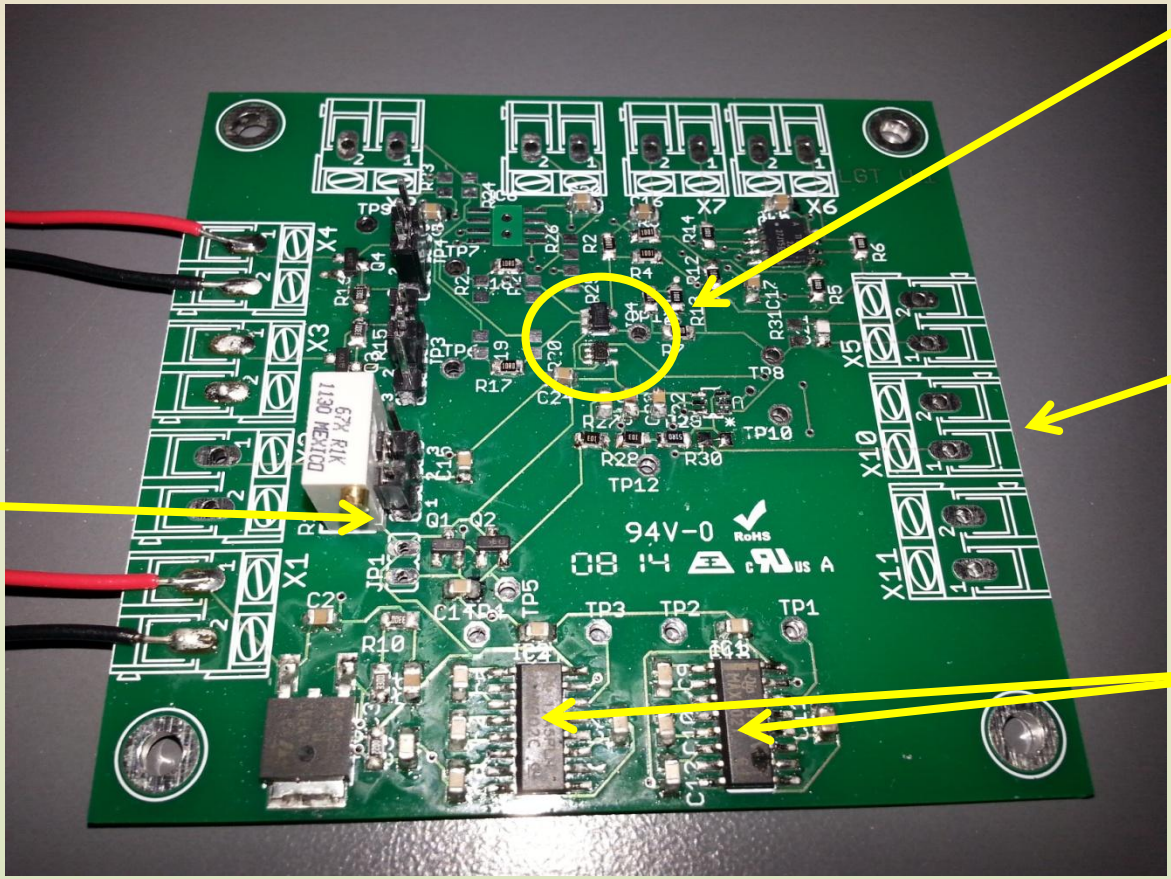
BITSTREAM

VARIABLE
SUPPLY
VOLTAGE

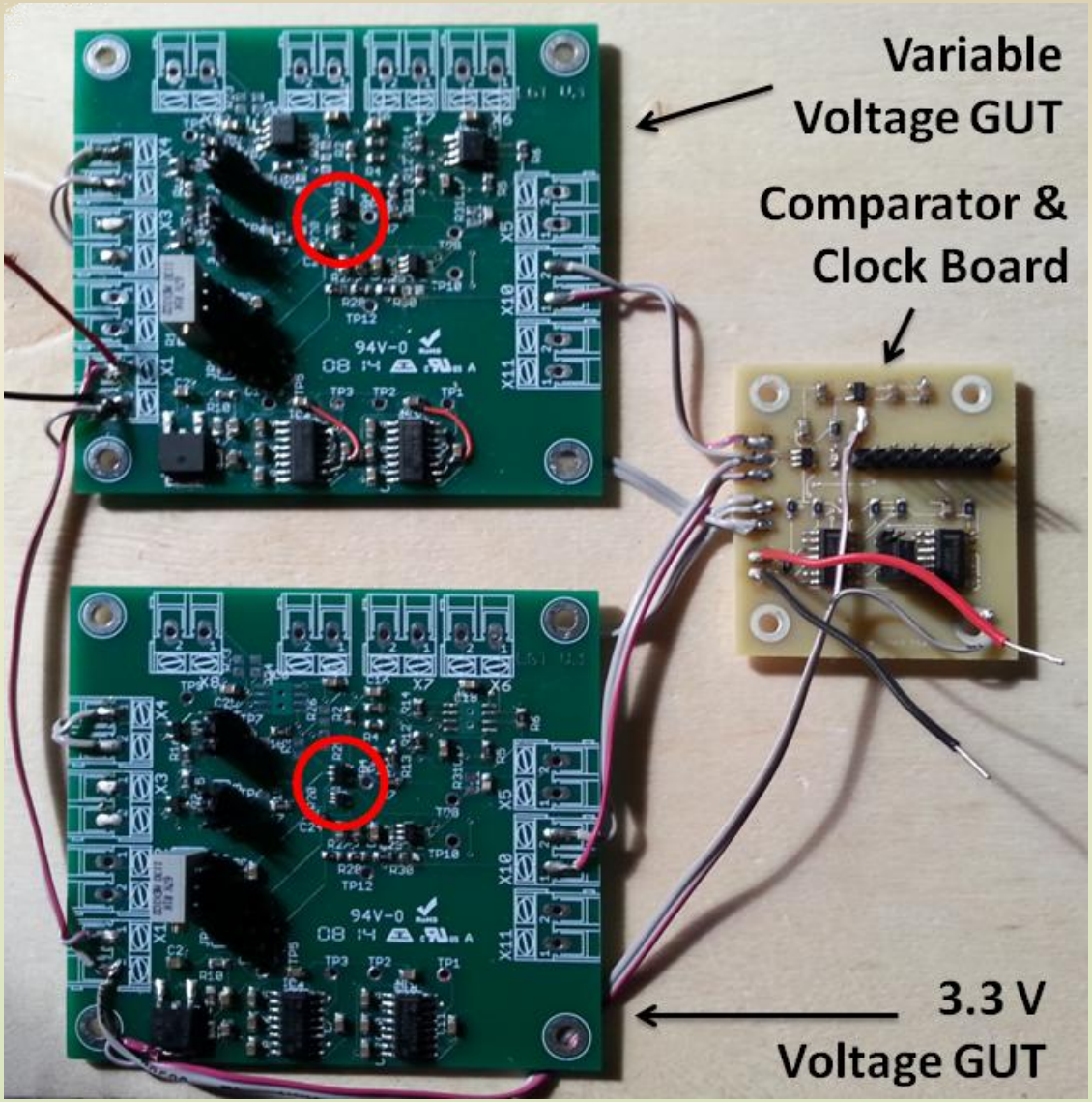
POWER SUPPLY

EXIT TO THE
COMPARATOR

VOLTAGE
SUPPLY TO THE
I/V
CONVERTER



View of the complete system



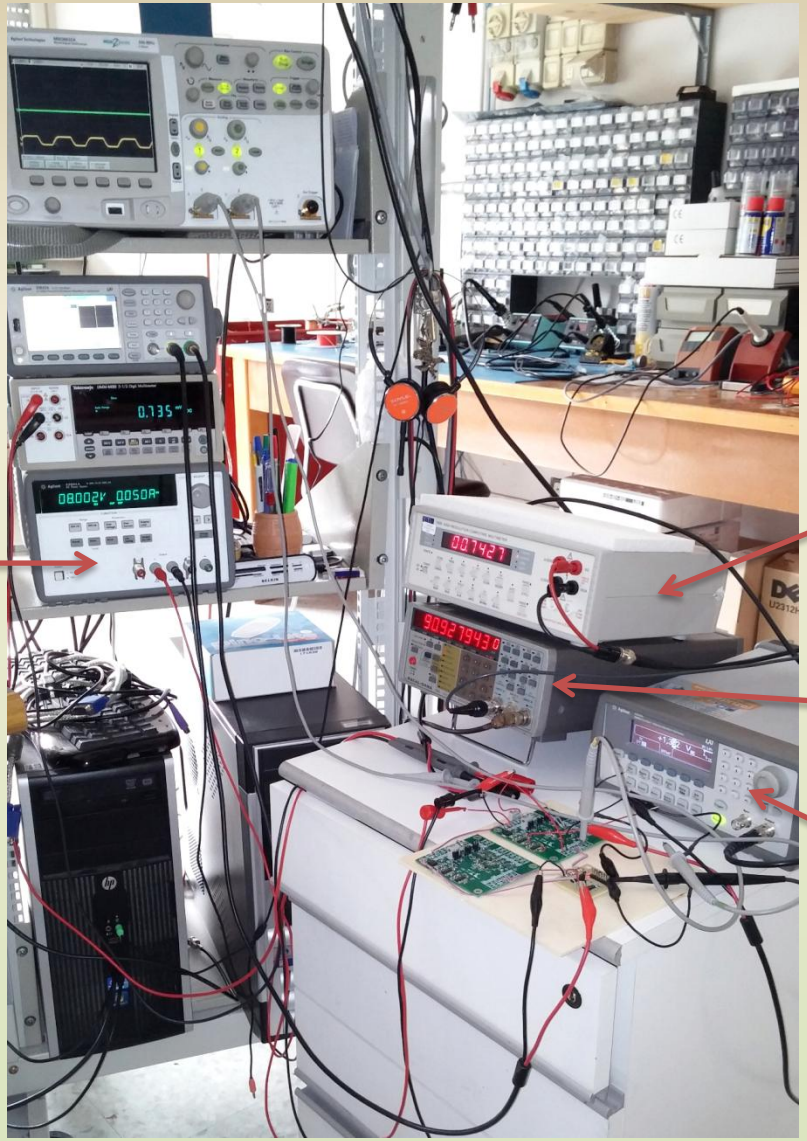
View of the test setup

2 Ch. Oscilloscope

2 Ch. Signal generator

Multimeter

Power Supply



Multimeter

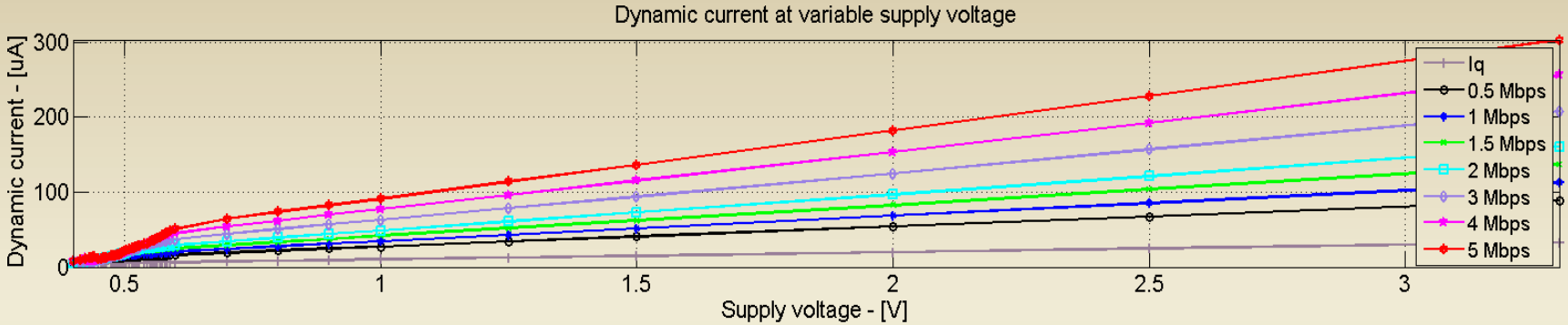
Universal counter

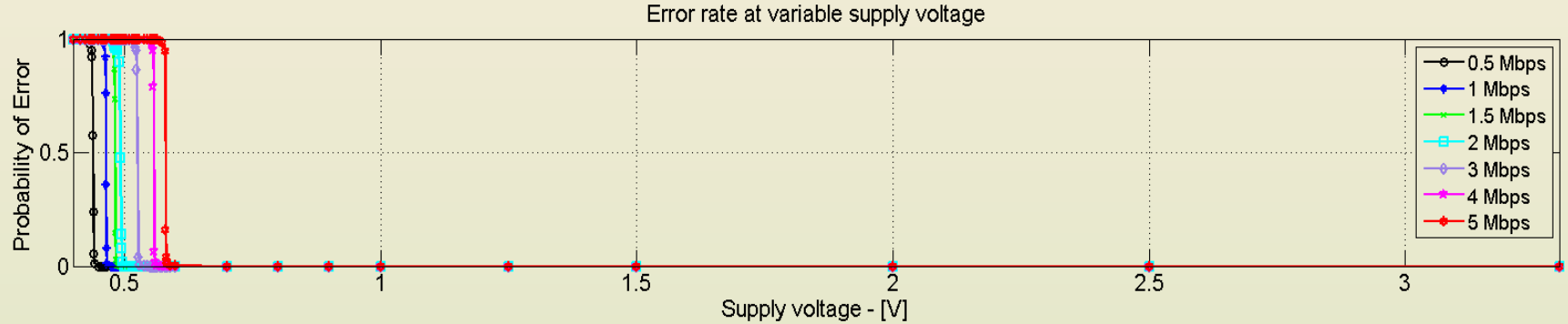
1 Ch. Signal generator

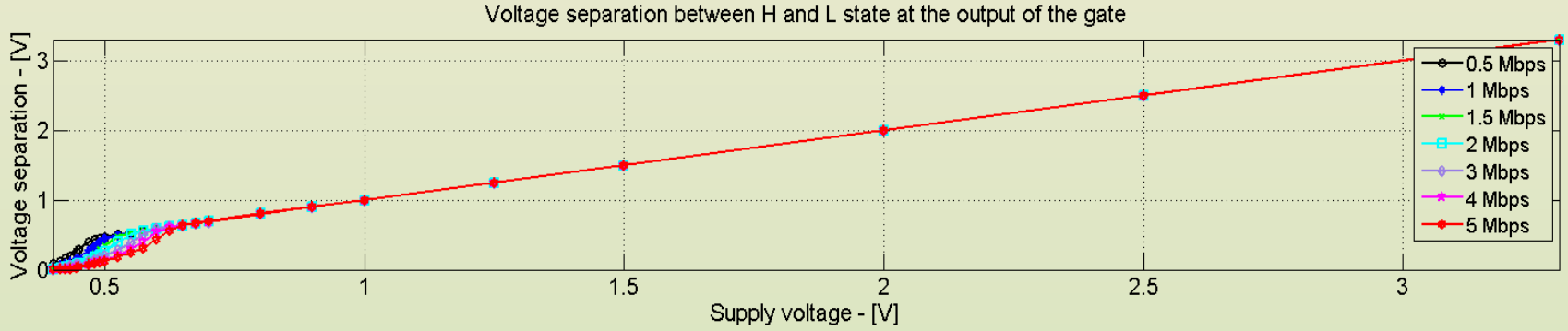
Current and error detection measurement procedure

1. Set the reference voltage to power the NAND gate at 0.4 V
2. Set the bit generator to have 0.5 Mbps (0.5 MHz square wave)
3. Read the current required by the NAND
4. Read the error amount on the digital counter
5. Increase the bit rate
6. Repeat the steps 3 to 5 until 5 Mbps bit rate has been reached
7. Slowly increase the supply voltage (ex. 10 – 20 mV steps)
8. Repeat the steps 2 to 7 until the 3.3 V supply voltage has been reached

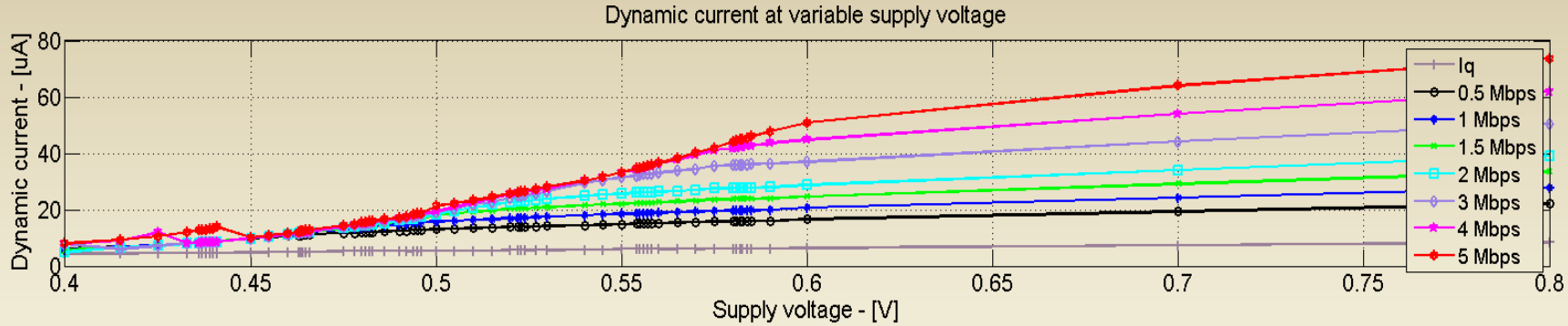
Measurements

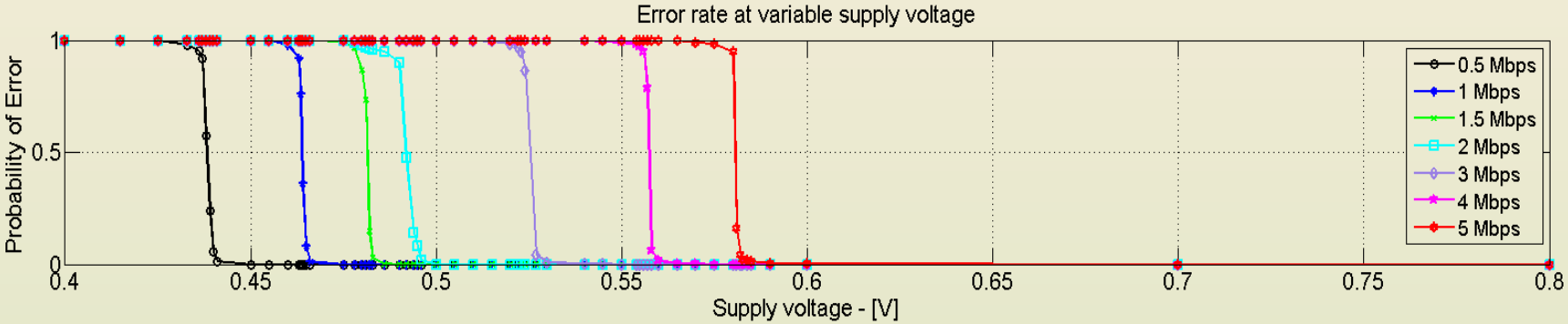


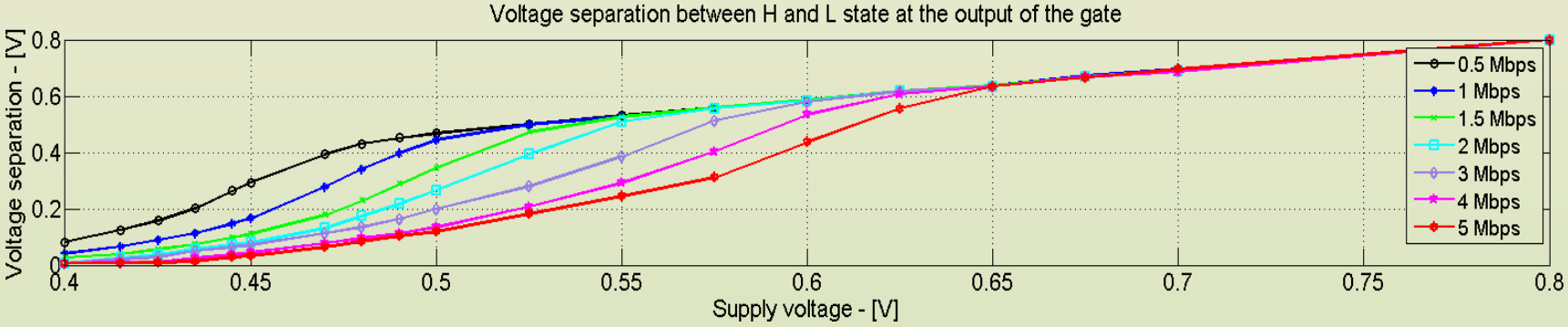




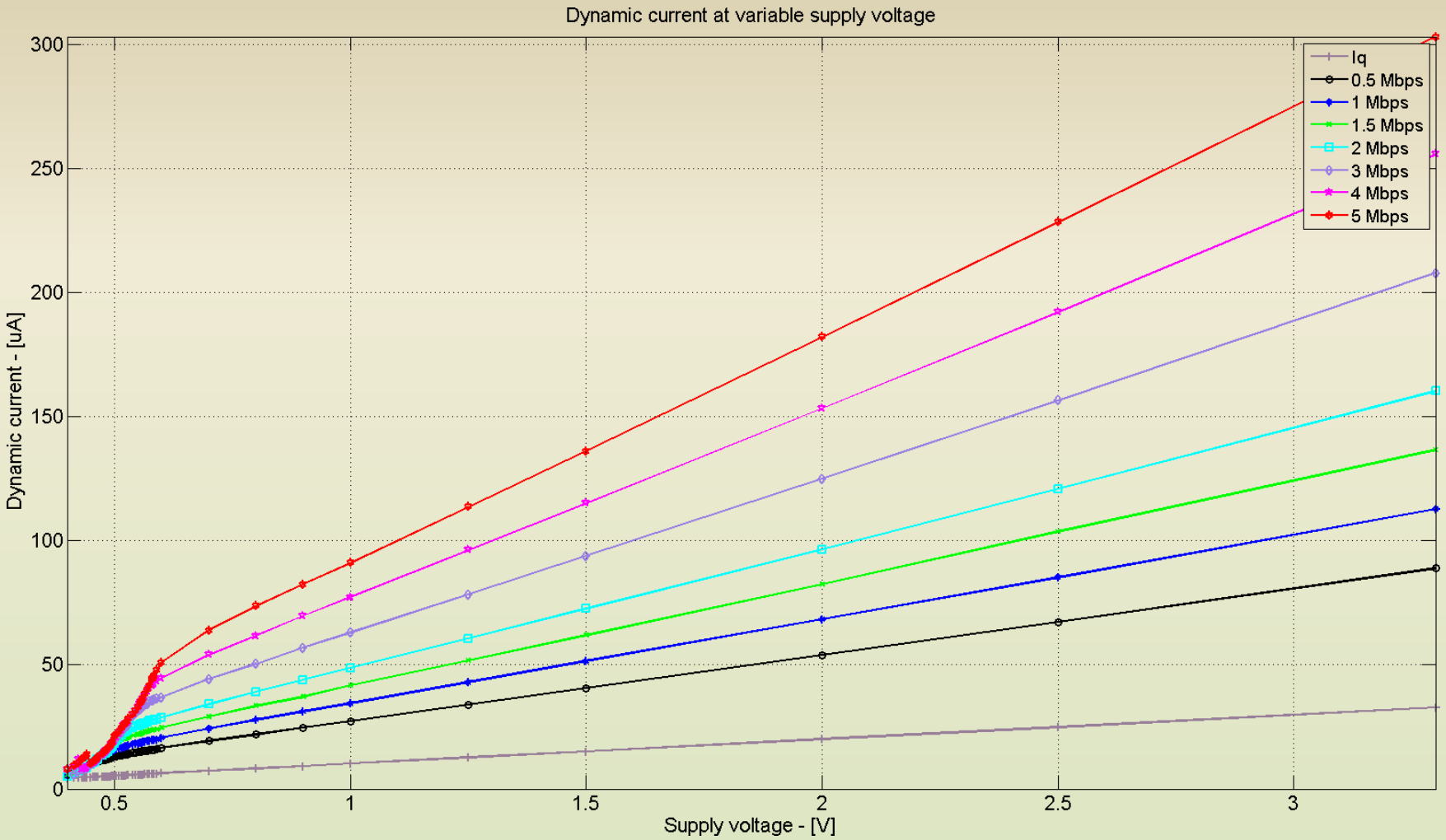
Measurements (0.4 V - 0.8 V)



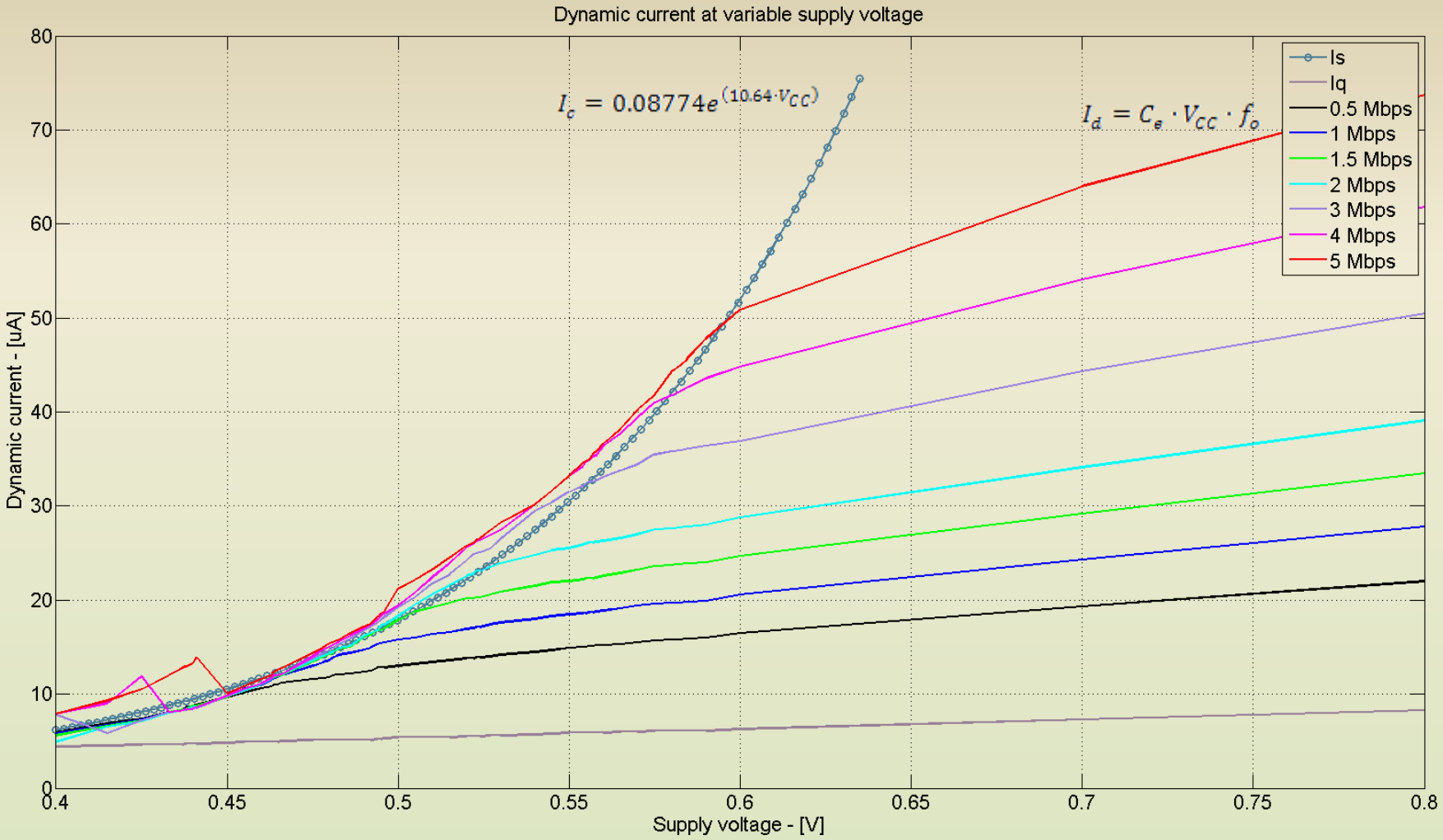




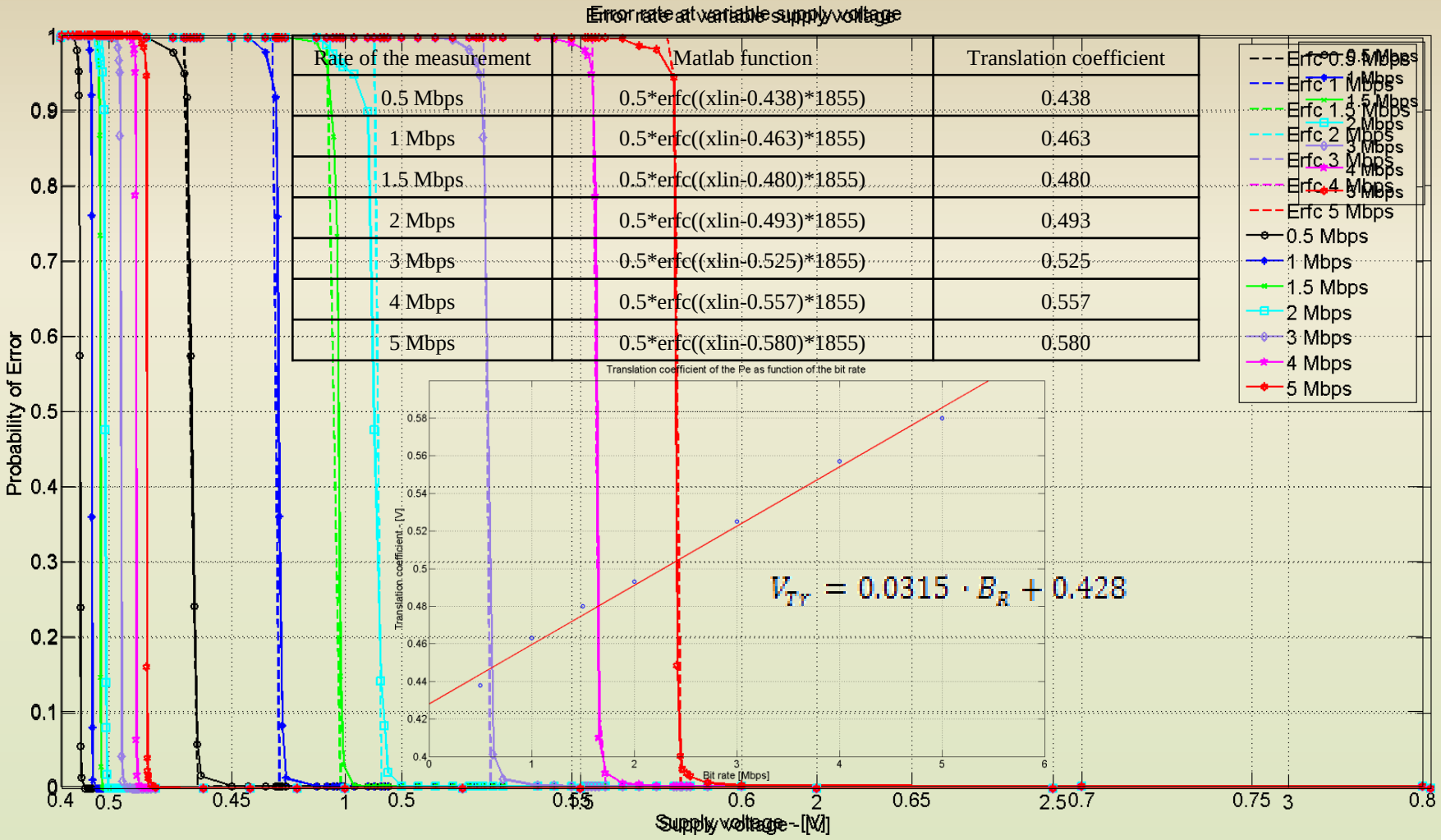
Dynamic current measurements



Dynamic current measurements (0.4 V – 0.8 V)

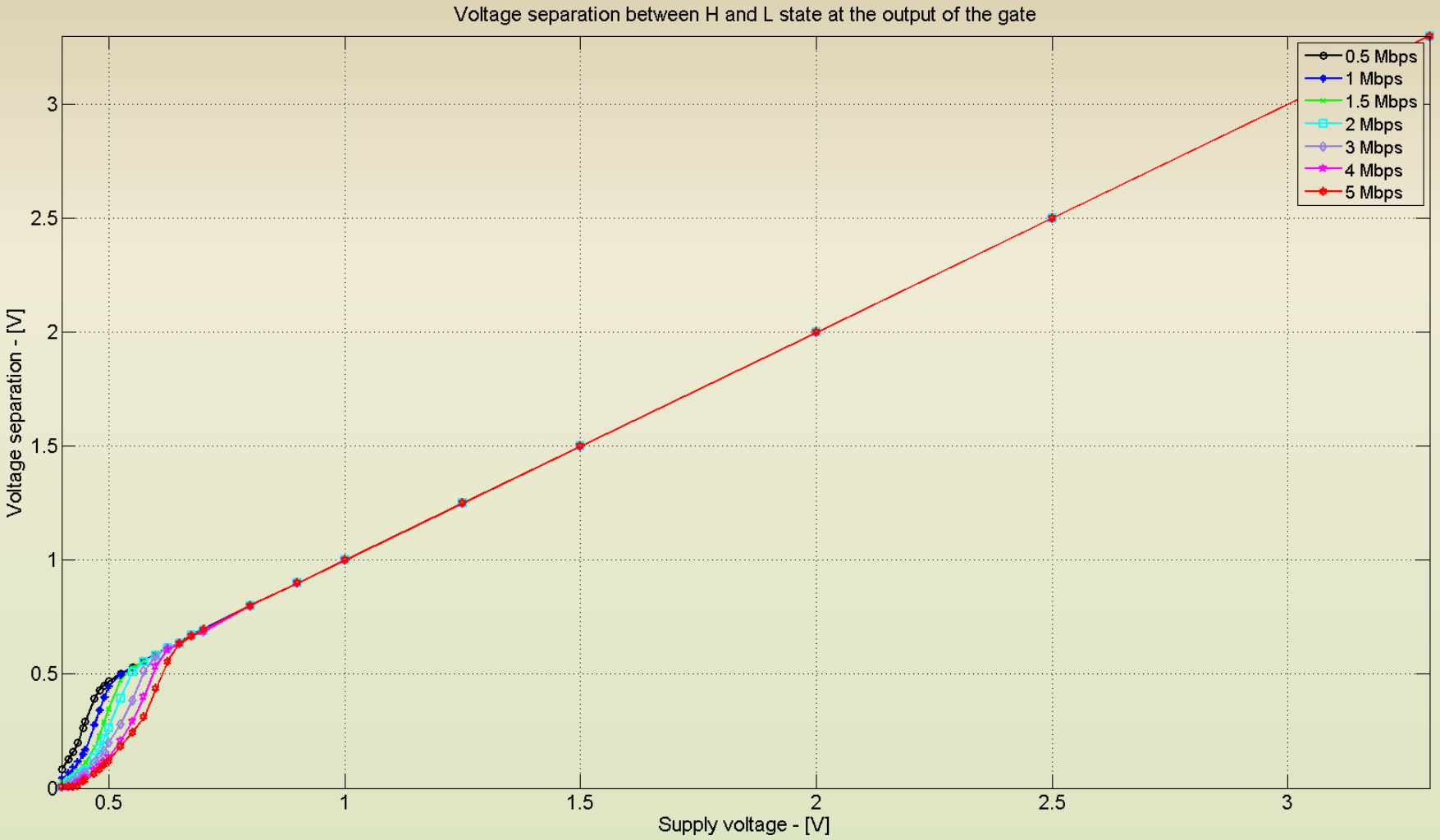


Error rate measurements

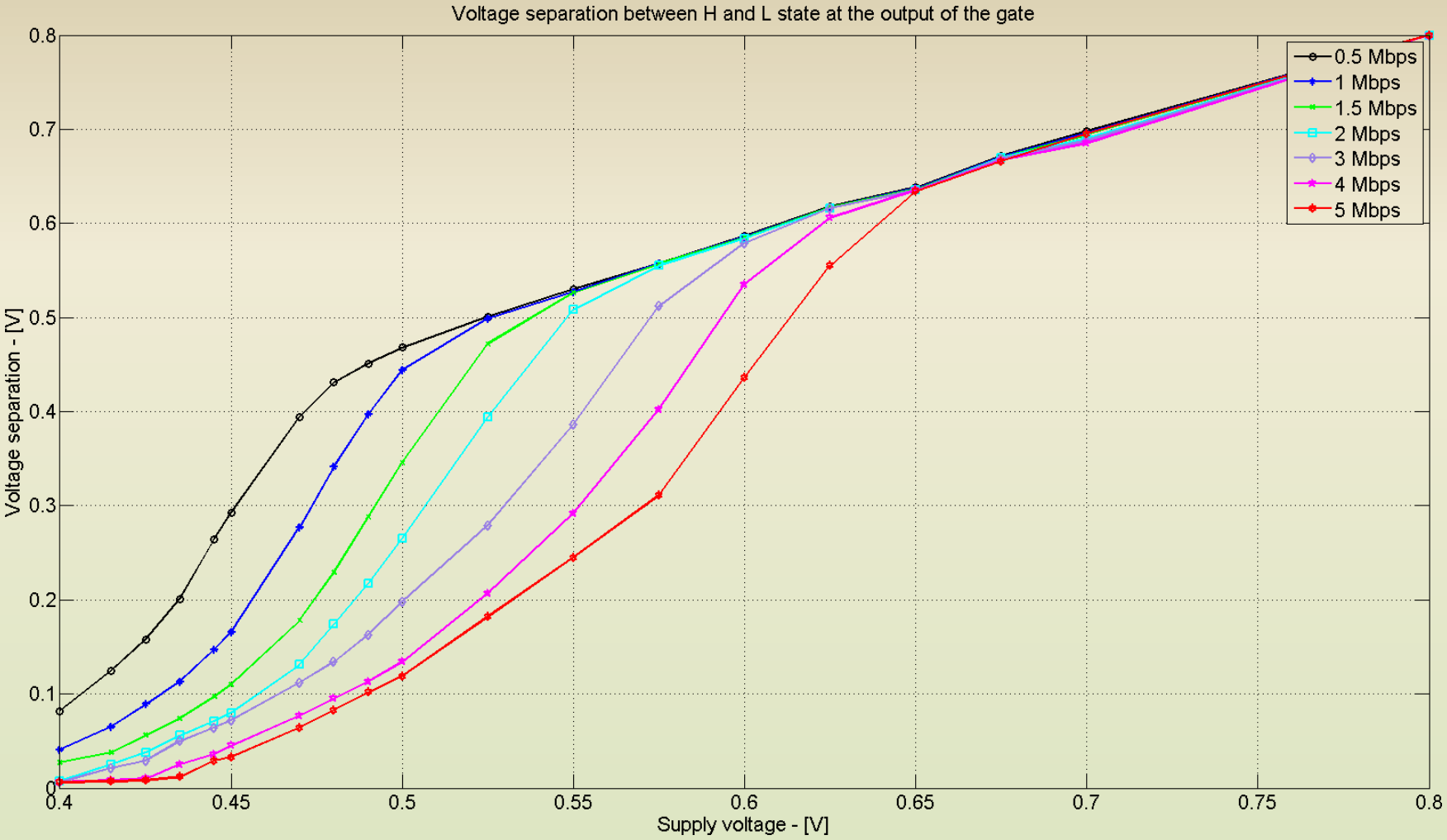


Rate of the measurement	Matlab function	Translation coefficient
0.5 Mbps	0.5*erfc((xlin-0.438)*1855)	0.438
1 Mbps	0.5*erfc((xlin-0.463)*1855)	0.463
1.5 Mbps	0.5*erfc((xlin-0.480)*1855)	0.480
2 Mbps	0.5*erfc((xlin-0.493)*1855)	0.493
3 Mbps	0.5*erfc((xlin-0.525)*1855)	0.525
4 Mbps	0.5*erfc((xlin-0.557)*1855)	0.557
5 Mbps	0.5*erfc((xlin-0.580)*1855)	0.580

H-L level voltage separation measurements



H-L level voltage separation measurements (0.4 V – 0.8V)



Conclusions

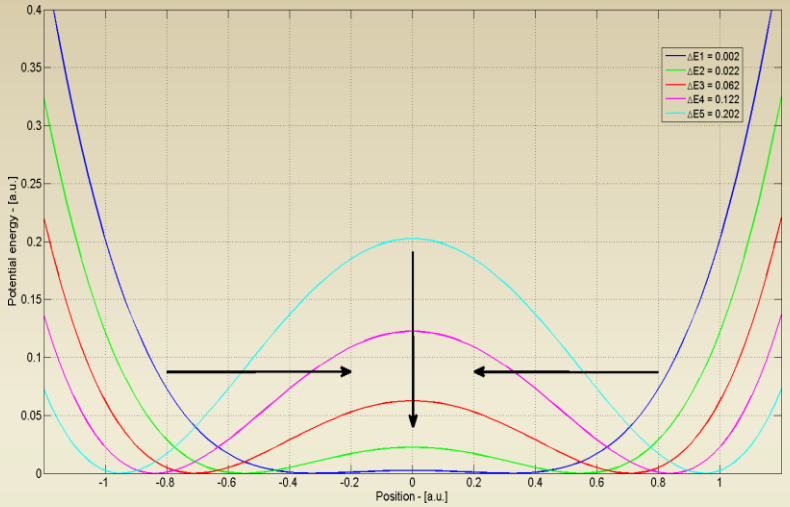
1. The overall current $I_{CC}(V_{CC})$ grows linearly for $V_{CC} > V_{T1}$, a threshold value that assumes different values for different bit rates BR, $V_{T1} = V_{T1}(BR)$.
2. For $V_{CC} < V_{T1}(BR)$ the overall current $I_{CC}(V_{CC})$ decreases almost exponentially with an exponent that is approximately the same for different bit rates.
3. The error probability $P_e(V_{CC})$ as a function of the supply voltage V_{CC}, decreases rapidly for $V_{CC} > V_{T2}$. V_{T2} assumes different values for different bit rates BR, $V_{T2} = V_{T2}(BR)$
4. For $V_{CC} < V_{T2}(BR)$ the error probability $P_e(V_{CC}) = 1$, it stays maximum regardless the value of the supply voltage, i.e. the response is totally random.
5. $V_{T1}(BR)$ is not necessarily equal to $V_{T2}(BR)$.
6. $V_{T1}(BR)$ and $V_{T2}(BR)$ grows approximated proportional with BR.
7. Absence of a step-like behavior for $V_{CC} = V_{T2}$. This seems to indicate the role played by the voltage/threshold fluctuations. In fact, in the absence of fluctuations, it can be expected the presence of a step-like change behavior of the error probability:
   $P_e(V_{CC}) = 0$ for $V_{CC} > V_{T2}$ and $P_e(V_{CC}) = 1$ for $V_{CC} < V_{T2}$.
   As it have been shown, this is not the case here, the error probability function looks like an exponential, far enough from a step-like behavior.

Thus the device failure should be considered as a stochastic phenomenon other than a deterministic event.

Conclusions

Realistic model of the two states of equilibrium

- particle in a bistable potential subjected to a force
- the distance between the two wells and the height of the barrier is supply voltage dependent
- the role of fluctuations can be taken into account by modeling the error probability $P_e(V_{CC})$ in terms of a threshold crossing probability by a stochastic process $s(t) = V_T(V_{CC}) + n(t)$, where $n(t)$ is an exponentially correlated, zero mean, Gaussian distributed noise and $V_T(V_{CC})$ is a threshold value function of the supply voltage V_{CC}



- given a threshold V_T, the error probability $P_e(V)$ can be expressed as the probability that the $P_e(V) > V_T$, where V_T is a function of the supply voltage V_{CC} and of the bit rate BR.

Power saving compared to the power required
at 0.8 V supply voltage for an error probability Pe = 0% and Pe=1%.

Bit Rate	Power Saving Pe = 0% @ V Supply	Power Saving Pe = 1% @ V Supply
0.5 Mbps	74.4 % @ 0.450 V	77.2 % @ 0.445 V
1 Mbps	72.4 % @ 0.475 V	75.0 % @ 0.466 V
1.5 Mbps	70.7 % @ 0.490 V	72.8 % @ 0.485 V
2 Mbps	68.5 % @ 0.505 V	72.3 % @ 0.498 V
3 Mbps	57.5 % @ 0.550 V	65.4 % @ 0.528 V
4 Mbps	52.3 % @ 0.575 V	57.3 % @ 0.573 V
5 Mbps	25.1 % @ 0.690V	53.2 % @ 0.587 V


Thank you!