TOLOP - Towards Low Power ICT

FET Proactive: Minimising Energy Consumption of Computing to the Limit

www.tolop.eu

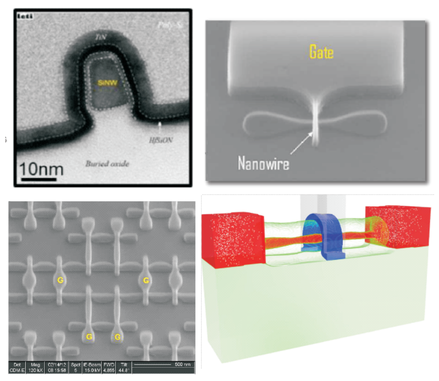
Aims of the Project

The TOLOP project comprises investigation into three of the levels necessary for a paradigm shift in low-power electronics:

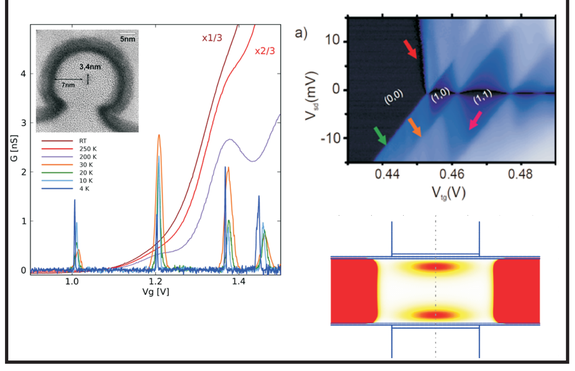
- **Fabrication and measurement of devices which are inherently low-power in switching operation at room temperature:**
  We study novel CMOS-compatible single-electron devices such as the single-electron transistor, single-molecule transistor and single-atom transistor. Moreover we explore novel reconfigurable spintronic devices.
- **Theory of specific device implementation for each of those technologies to explain and validate the principles behind their low-low power capabilities:**
  We explore both non-Boolean logic implementations, such as multi-valued and parallel logic,and optimised Boolean logic with the potential for exponential improvement in power needs.
- **Design of architecture to enable the circuit operation of these technologies for overall low-power circuit operation:**
  We investigate hybrid single-electrontransistor/transistor circuits for optimised circuit-level implementations and reduced power consumption.

Single Electron and Spintronics Devices

CMOS Trigate Transistors and Circuits



4K and Room Temperature Single Electron Effects



•Fabrication single-electron transistor and single-atom transistors using fully depleted SOI technology on 300 mm wafers.

•Fabrication of test circuits like ring oscillators and SRAM memory cells.

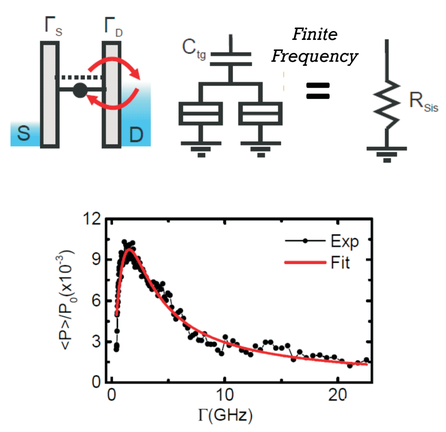
•Fabrication of reconfigurable single-electron spintronics devices

•Morphological characterisation

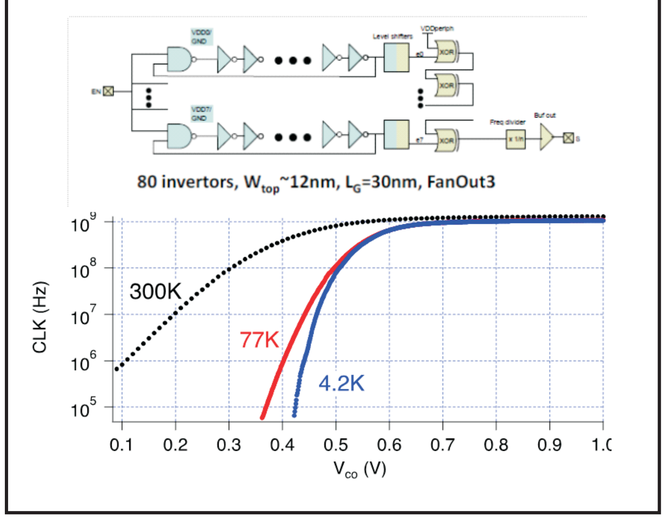
•Room temperature and low temperature device variability

Speed and Power Dissipation

Excess Dissipation on Single-Electron Devices at Finite Rate



Clock Speed at Room and Low Temperature



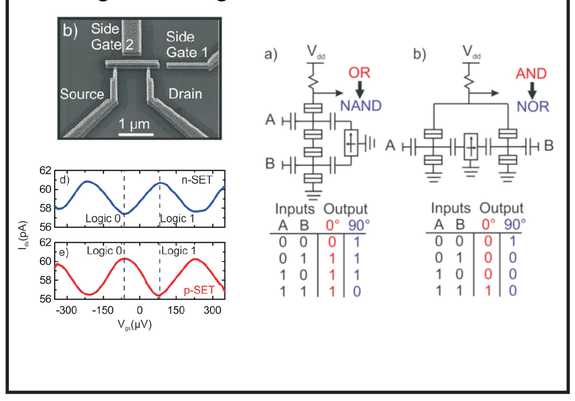
•Evaluation of dissipation on single-electron devices operated at high frequencies
  High-frequency resistance: Sisyphus resistance
  High frequency reactance: Tunneling Capacitance

•Evaluation of device clock speed and power dissipation per gate at room temperature and low temperature

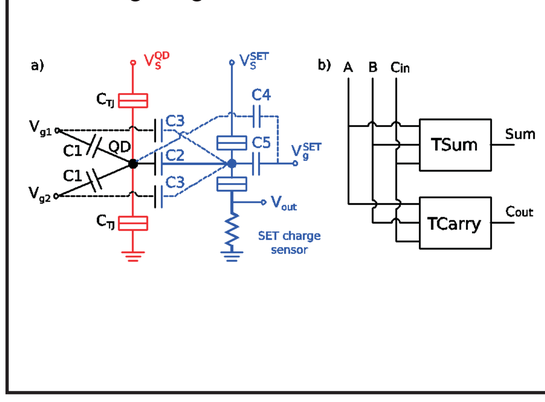
•Benchmark against state-of-the art CMOS technology

Complex Logic Implementation

Reconfigurable Boolean Logic using Magnetic Single Electron Transistors



Optimised Full Logic Addition using Single-Electron Transistors



•Design and modelling of the mode of operation of non-Boolean gates, circuits and cascade thereof on novel single electron devices

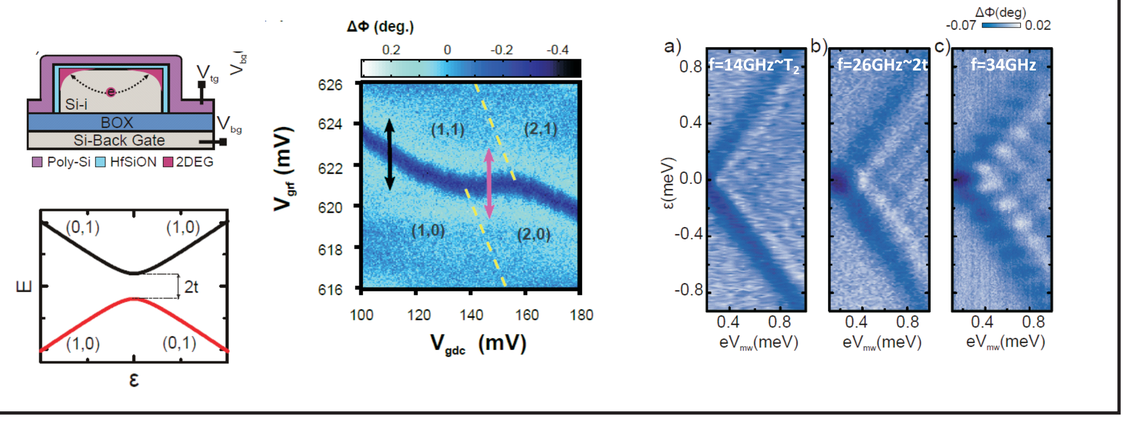
•Evaluate the fundamentals of operating a finite state machine on single electron devices

•Explore parallel logic on single electron devices

•Determination of an appropriate metric for energy consumption in information processing at a finite rate at the atomic scale

Towards Zero Power Consumption

Adiabatic Classical and Quantum Information Processing



•Investigate routes towards zero dissipation information processing using single-electron devices. We explore charge and spin coherence.

•Dissipation-less single electron transfers using CMOS single electron devices

•Single charge and spin detection with high sensitive techniques

•Ultrafast charge manipulation f > 40 GHz and coherent control

References

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Partners

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Coordinator Details

M Fernando Gonzalez-Zalba, mg507@cam.ac.uk, David A Williams, daw61@cam.ac.uk